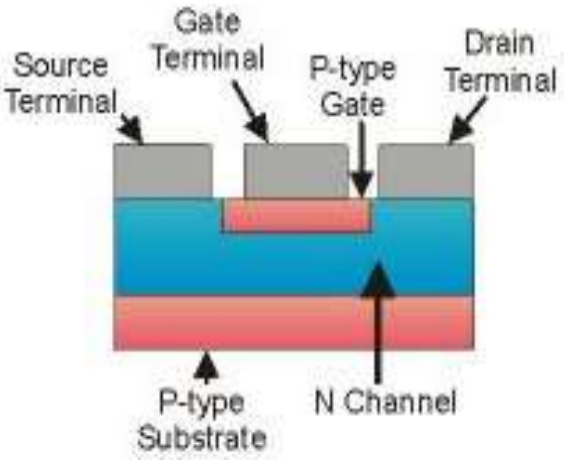
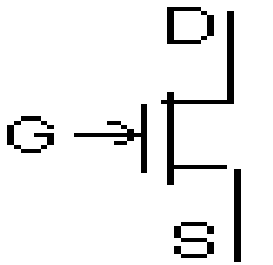
Field Effect Transistors

LECTURE NO. - 41

Field Effect Transistors

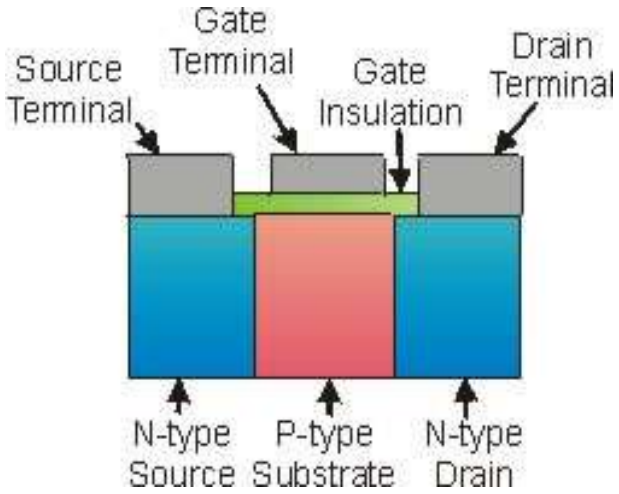
JFET

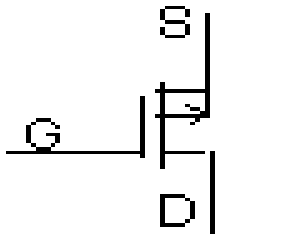




JFET

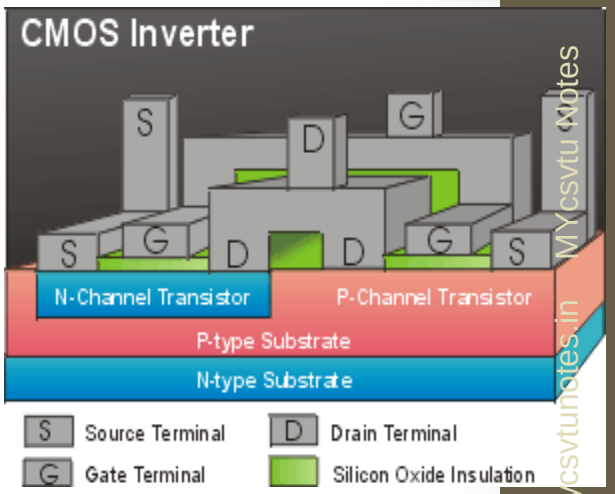
MOSFET

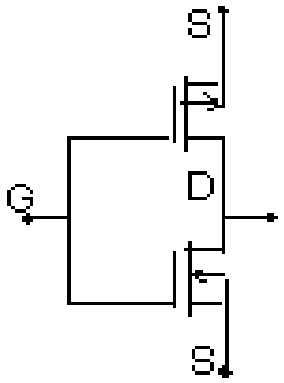




P-channel MOSFET

CMOS





Field Effect transistors - FETs

First, why are we using still another transistor? BJTs had a small problem - the input signal was a current I_B which was small but not that small. This was the control signal. Typically we would prefer that we control with a voltage directly.

This has an added benefit. If the device control only depends on a voltage signal we can design it so it draws little or NO current! This means that when we attach it to something like a thermocouple, it will not disturb the input since it is drawing no power. In other words the input impedance of the circuit is large.

Comparison :

FET	BJT
Gate	Base
Drain	Collector
Source	Emitter
Gate Voltage	Base current
Drain current	Collector current
Drain-source voltage	Collector-Emitter Voltage

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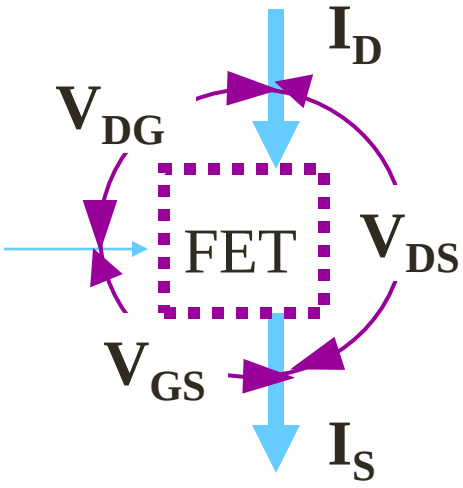
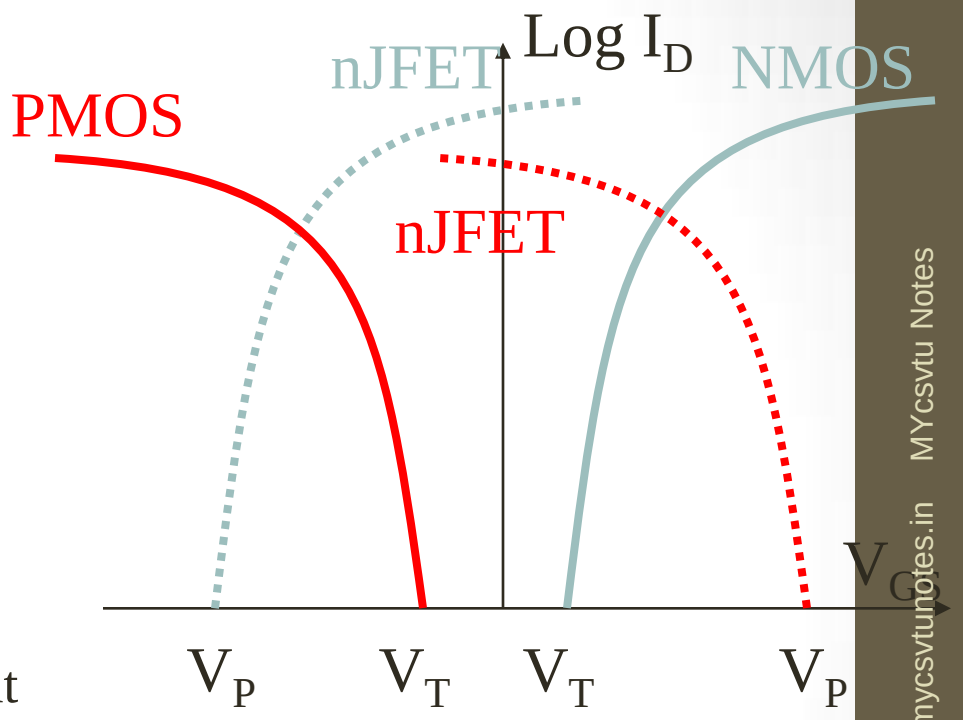
Flavors of FETs

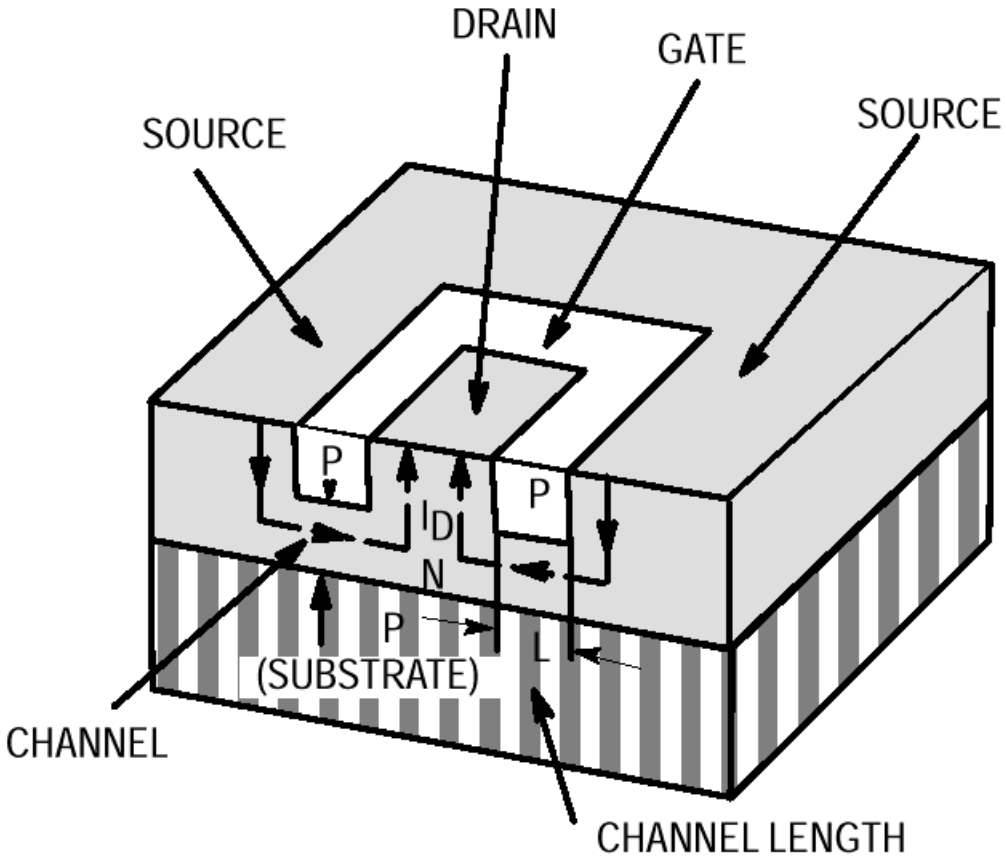


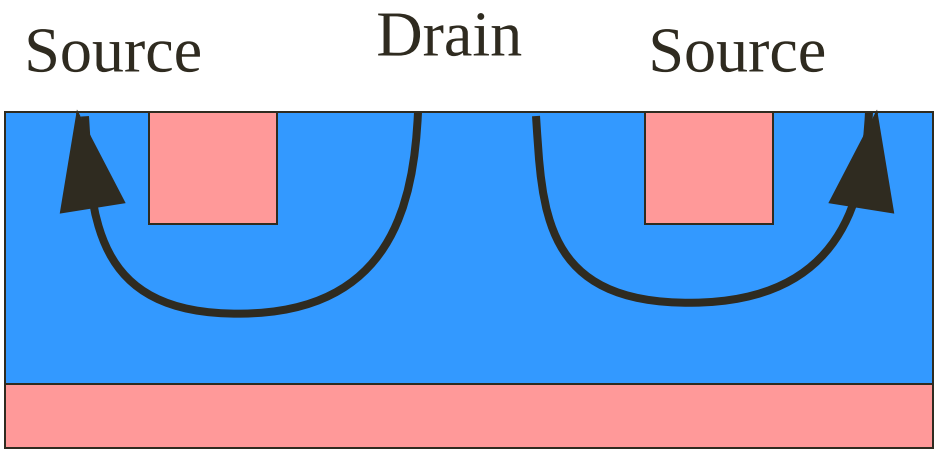
The basic way to think of an FET is that there is a current $I_D = I_S$ that is flowing through a channel that is controlled by a voltage V_{GS}. Since the channel offers resistance to the flow it has a voltage drop V_{DS}. These three parameters completely characterize the device.



The above shows difference between different types of FETs. The important thing to note is that the shapes are the same! We will focus on the blue curves, where electrons are the carriers.

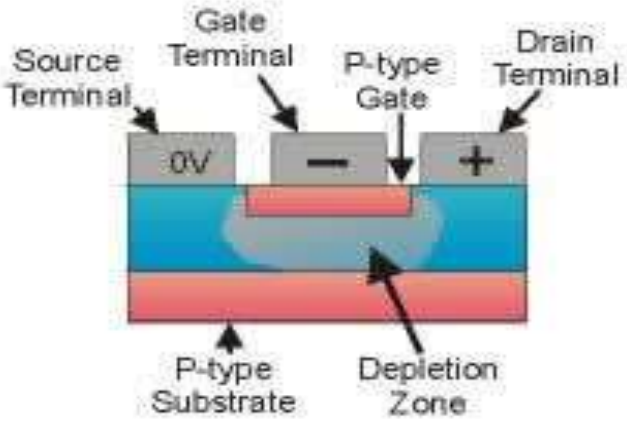
Junction FETs





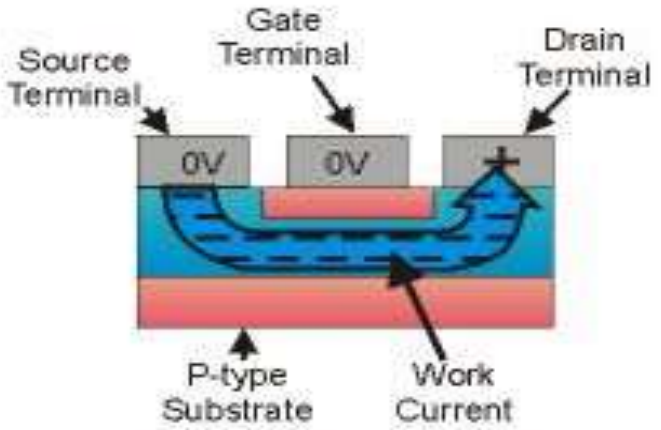
The arrows show current flow from the drain to source.

How a JFET transistor works?



N-channel JFET Off

When the gate is negative ,it repels the electron in the N-channel. So there is no way for electrons to flow from source to drain.



N-channel JFET On

When the negative voltage is removed from Gate ,the electrons can flow freely from source to drain .so the transistor is on.

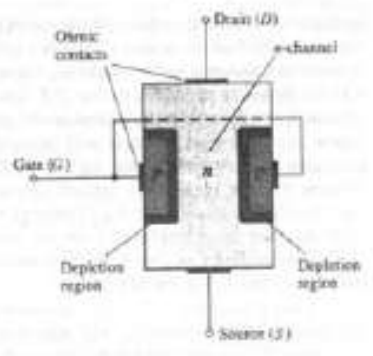
Junction Field Effect Transistors - JFET

Major part is *n*-type material channel, embedded between two *p*-type material.

Two ends of the *n*- type material channel are Drain (D) and source (S)

Two *p*-type material are connected together and referred as Gate (G)

Two *pn* junctions, depletion region at each junction



Junction Field Effect Transistors - JFET

V_{GS} = 0 v and V_{DS} some positive value

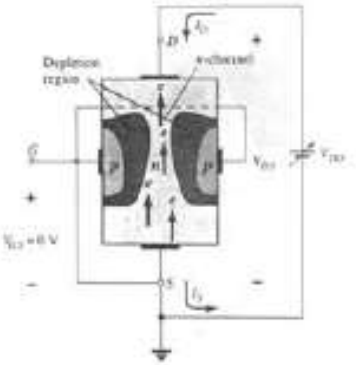
Gate and Source are same potential

Electrons will flow from source to drain as in *n* type semiconductor

$I_D = I_S$

Resistance of *n*-channel acts between drain and source

Depletion region is wider near the top of *p*-region



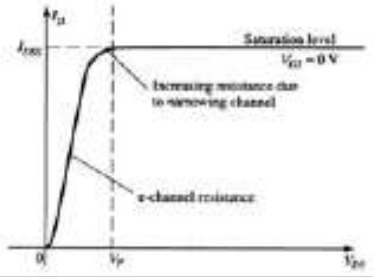
Junction Field Effect Transistors - JFET

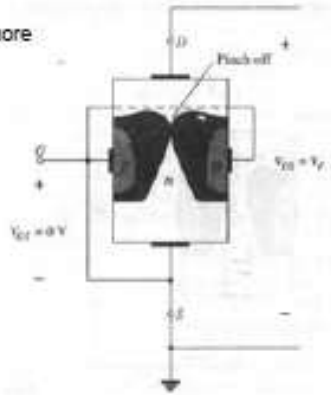
Initially it follows Ohm's law (almost straight line)

Later depletion layer widens

Pinch off level - depletion layer cannot increase more (very high resistance)

Give a feeling I_D will be zero. This is not possible



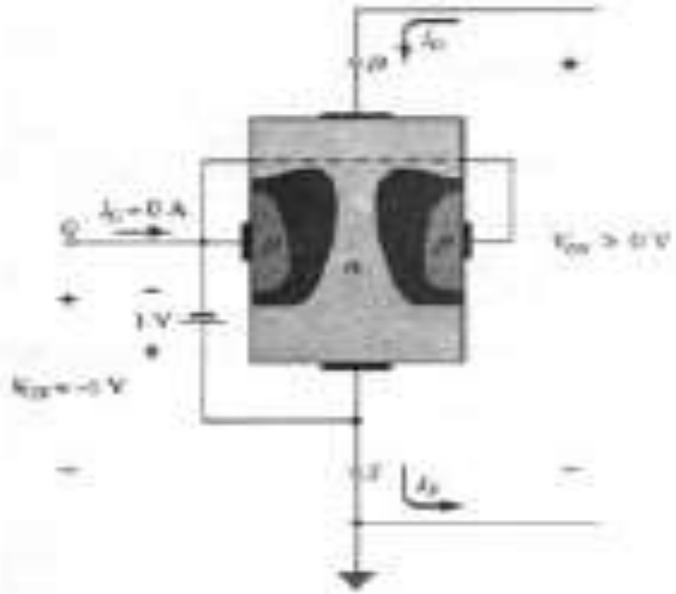


Junction Field Effect Transistors - JFET

V_{GS} < 0 v and V_{DS} some positive value

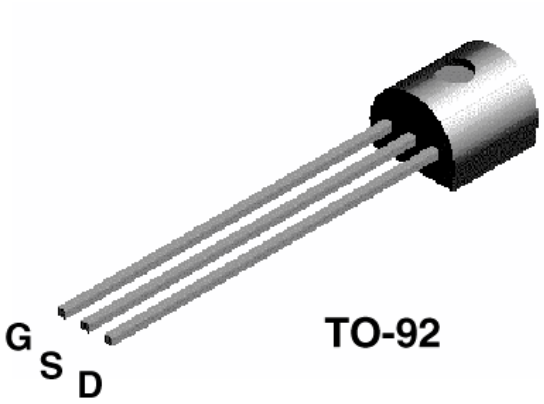
Gate to source voltage non zero

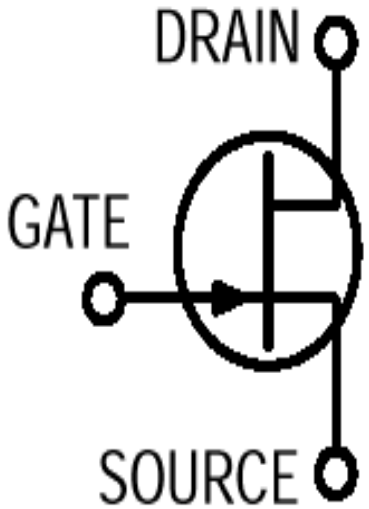
V_{GS} < 0 v more reverse bias and hence reduces saturation level for I_D. This will further reduce with reduction in V_{GS}



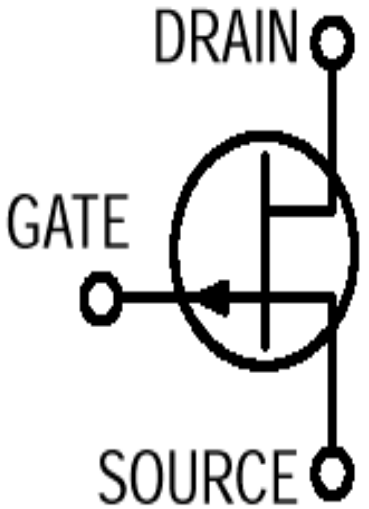
Junction FETs

2N5457
2N5458
2N5459





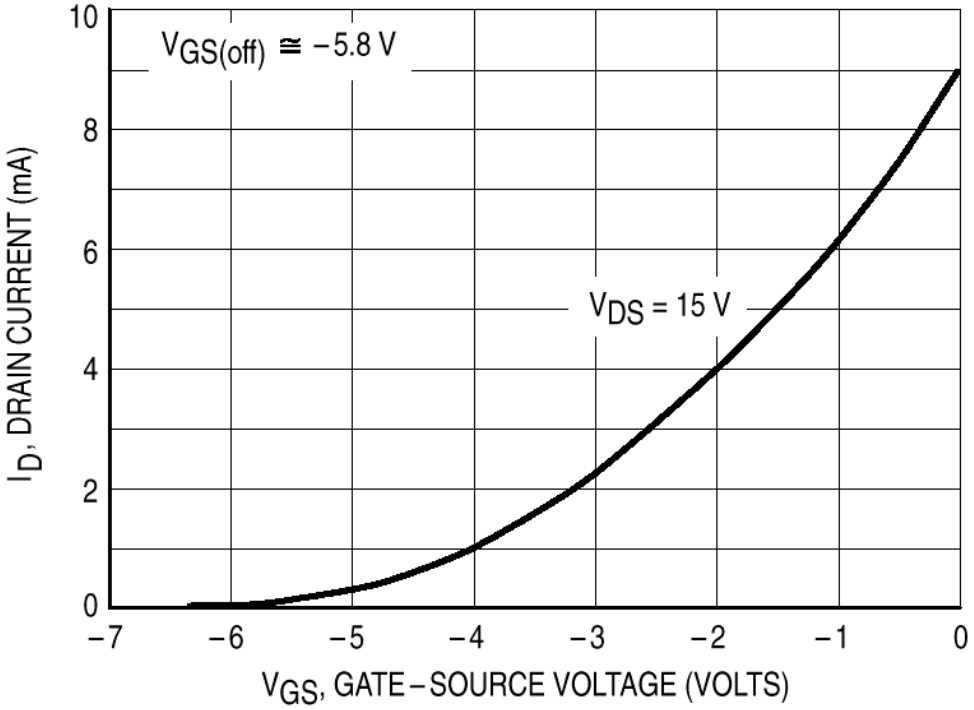
N-CHANNEL JFET



P-CHANNEL JFET

- LECTURE NO. – 43

Junction FETs - characteristic curves



Here we see the results of make the GS junction more reverse biased. This is a parabola given by

$$I_D = k(V_{GS} - V_P)^2$$

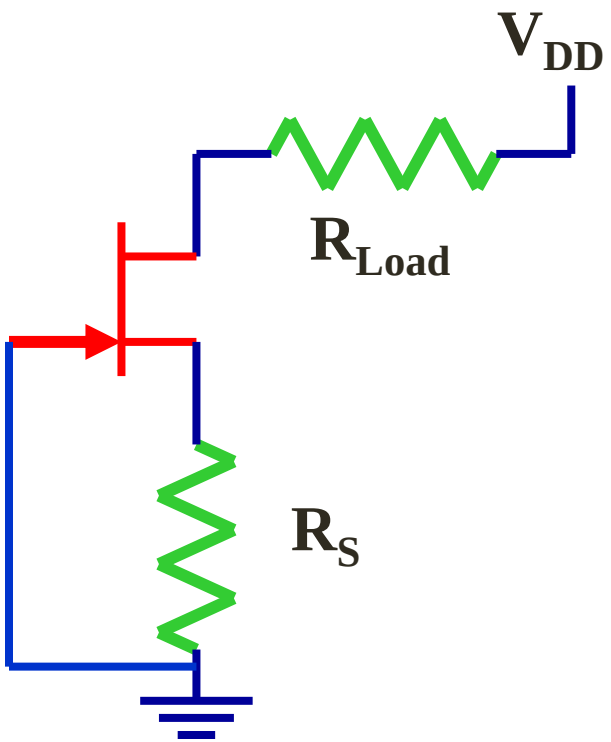
where k is a constant and VP is the pinch-off or threshold voltage. Note that the curve extends only to zero volts. This is because the junction is normally only reverse-biased to prevent damage if large current flow through the GS junction.

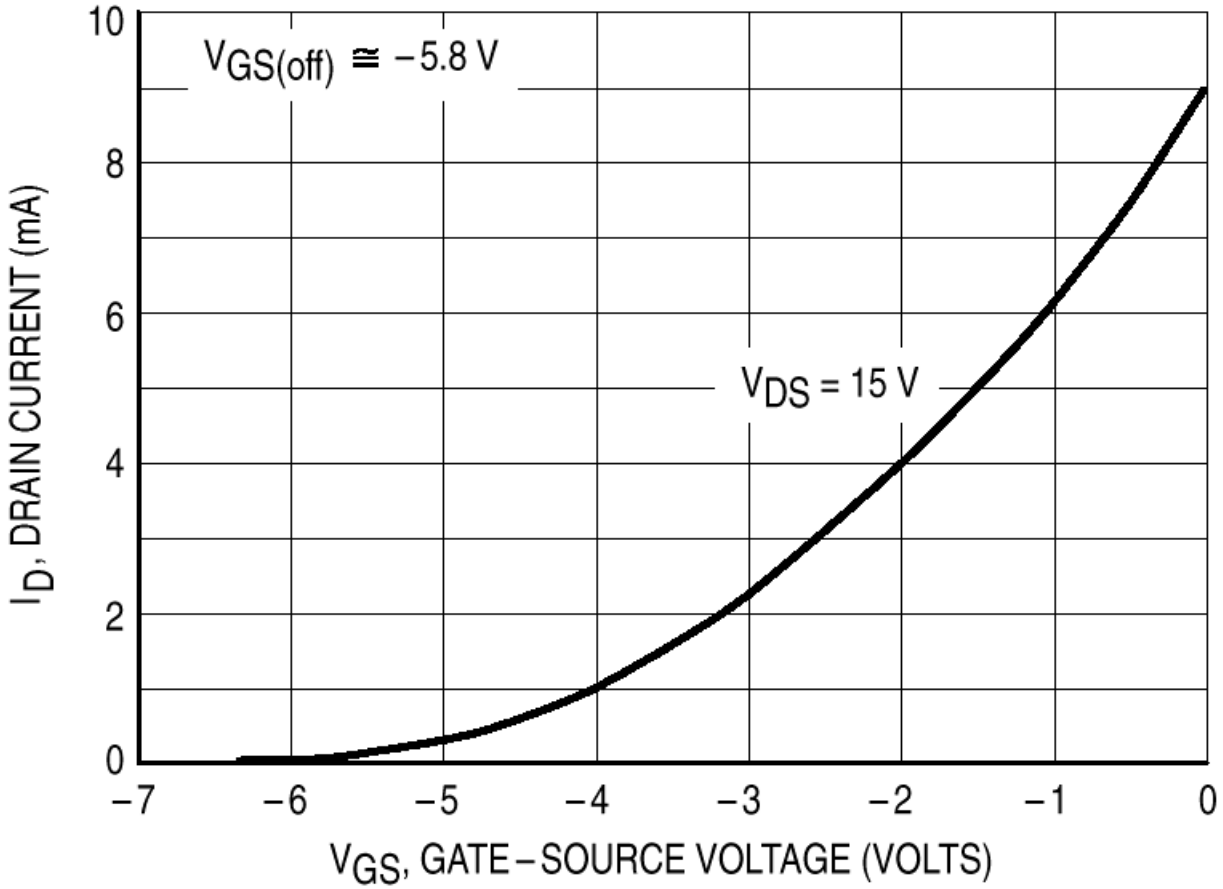
Regions of JFET operation:

- **Cut-off region:** The transistor is off. There is no conduction between the drain and the source when the gate-source voltage is greater than the cut-off voltage. ($I_D = 0$ for $V_{GS} > V_{GS}$,off)
- **Active region (also called the Saturation region):** The transistor is on. The drain current is controlled by the gate-source voltage (V_{GS}) and relatively insensitive to V_{DS}. In this region the transistor can be an amplifier.

- **Ohmic region:** The transistor is on, but behaves as a voltage controlled resistor. When V_{DS} is less than in the active region, the drain current is roughly proportional to the source-drain voltage and is controlled by the gate voltage.

Junction FET - current source





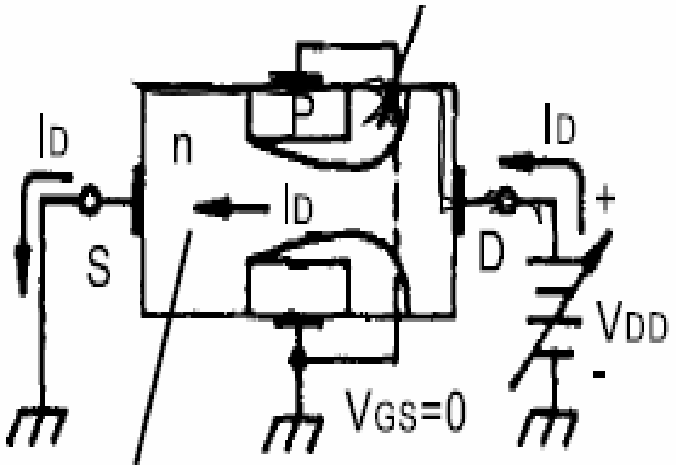
- The curve is not effected much by the value of VDS unless it gets too small. This means that we can apply a voltage to the gate and get exactly the same current for very different voltage drops across DS channel. The circuit above is a self-biased voltage controlled current source. If RS is 4k, then from the plot above 1 mA will flow resulting in VGS = -4 V. Regardless of the value of Rload (within the limits of the power supply VDD) exactly 1 mA will be delivered.
- The only downside of this circuit is that the load is not grounded on either end, but that can be fixed.

Common Specifications.

- ***I*DSS** is the drain current in the active region for *V*GS = 0. (*I*D source shorted to gate)
- ***V*GS,off** is the minimum *V*GS where *I*D = 0. *V*GS,off is negative for *n*-channel and positive for *p*-channel..
- ***g*m** is the transconductance, the change in *I*D with *V*GS and constant *V*DS.

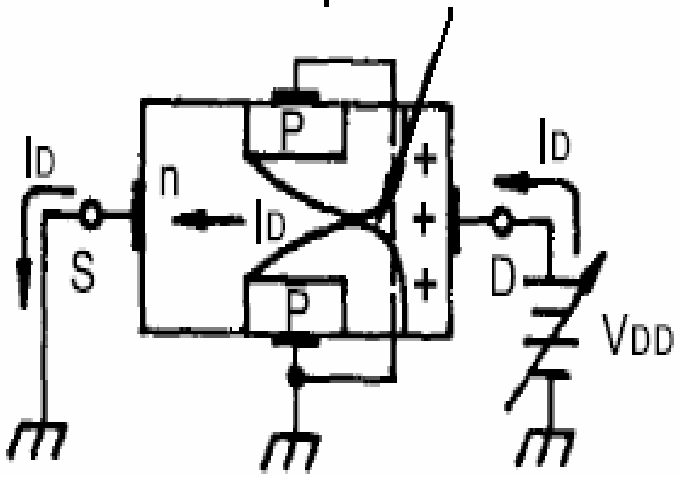
- When Vgs = 0, the relation between Vds and Ids is shown in Fig below.From this figure we can clearly view that Id will be increased with Vds until it maintains at a constant value. This constant value is called Idss, wherein the footnote “ds” means the current from drain to source, and the last “s” means it is under the status that drain-gate are short-circuit (Vgs = 0).

Depletion region
under reverse bias

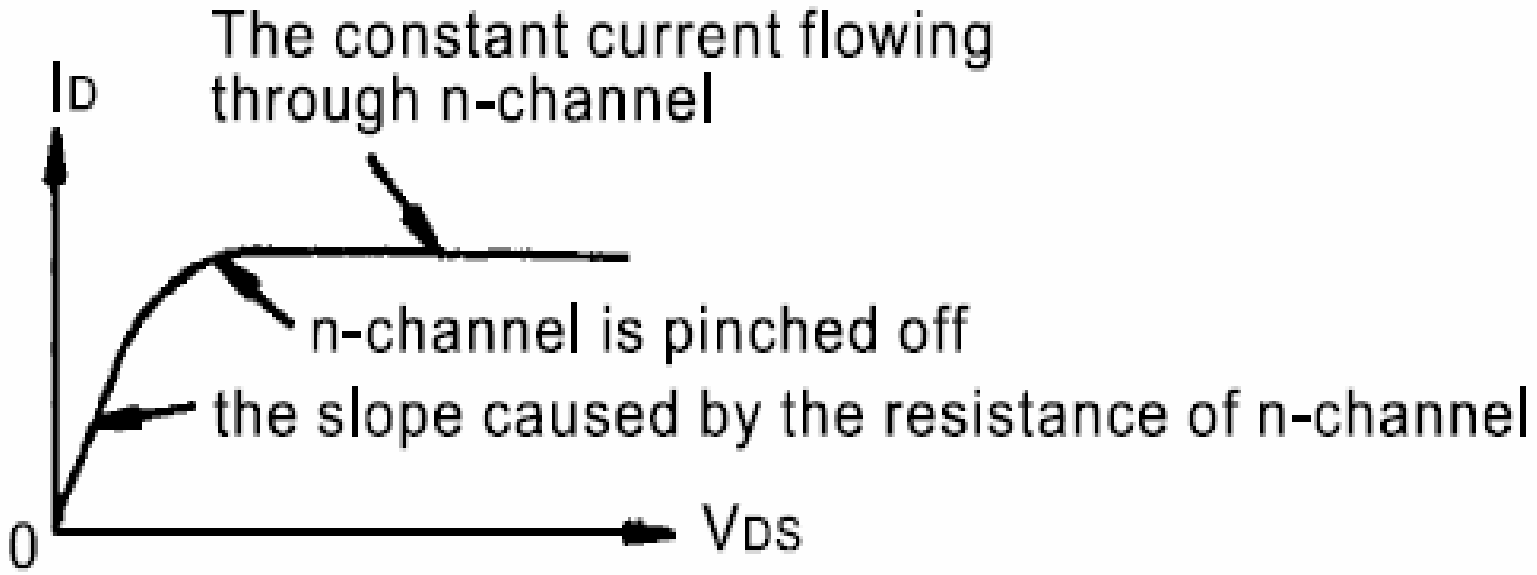


the current flowing
through channel

When the depletion region is
filled with the channel, the
channel is pinched off

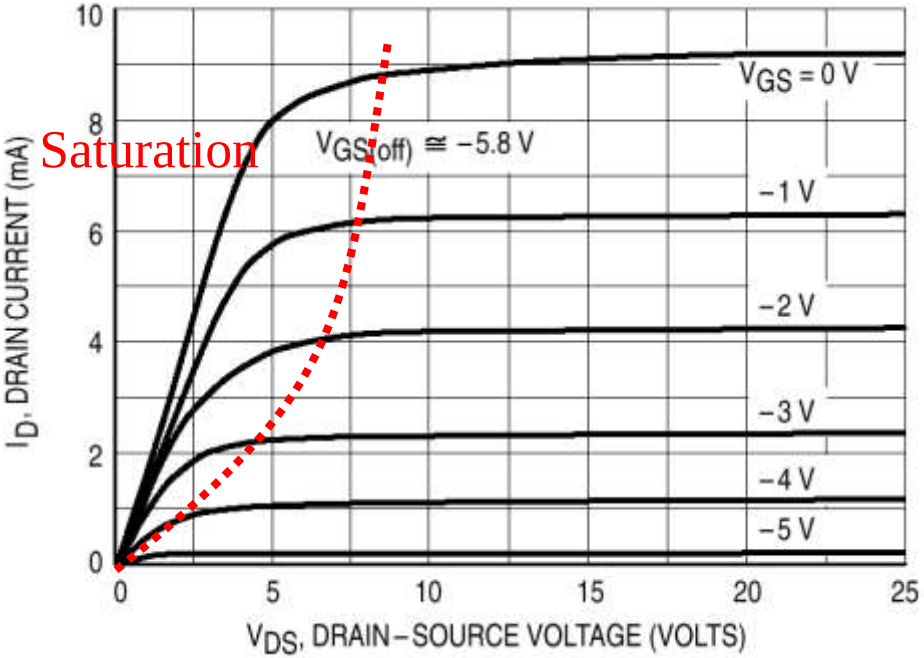


Pinch off voltage :



Junction FETs - characteristic curves (2)

Linear



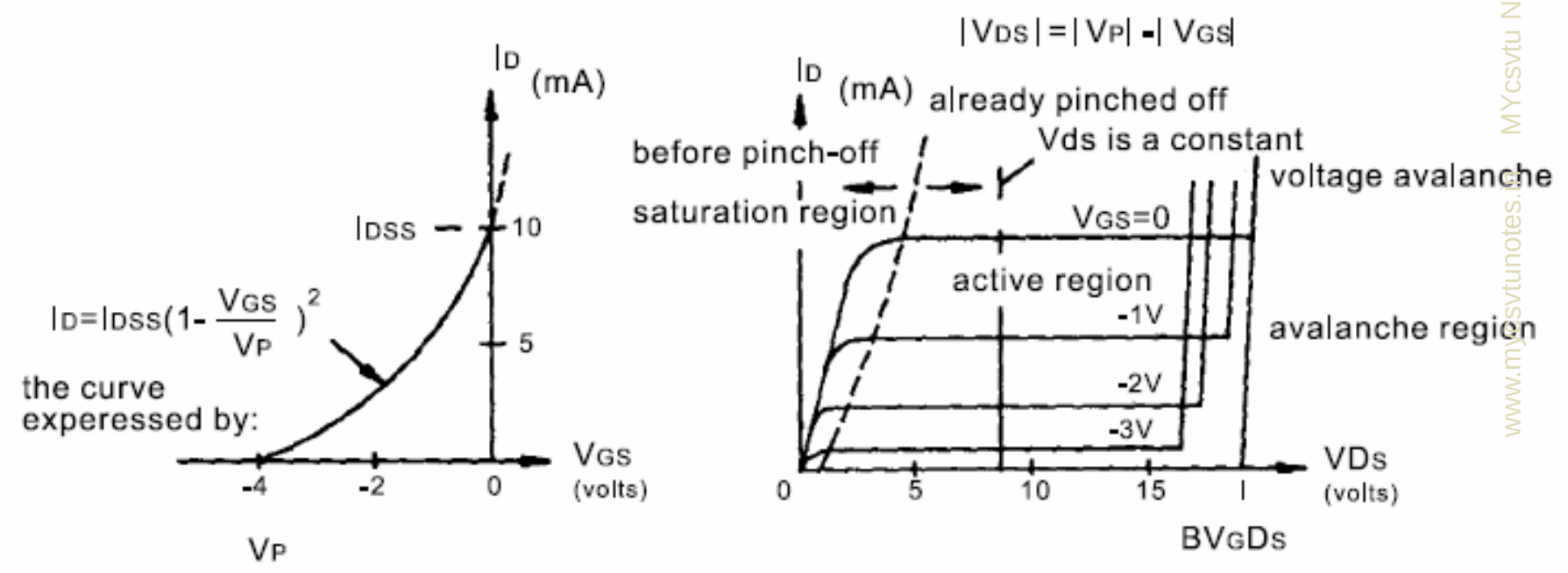
Linear $$I_D = k(V_{GS} - V_P)^2$$

Saturation $$I_D = 2k\left[(V_{GS} - V_P)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Like the BJT there are two regions of operation - saturation and linear (also called triode). Amplifier applications live in the saturation region; switching and variable resistor applications live in the linear region.

Although we will not discuss amplifiers, note that the drain current is dependent on VGS in a linear fashion and could be used to make a circuit with voltage gain.

Transfer Characteristic Curve



- Another characteristic curve for JFET is transfer characteristic curve. This is a variation curve of drain current Id corresponding to gate-source voltage Vgs while the drain-source voltage Vds is constant.
- Two points, Idss and Vp are the most important points in this transfer characteristic curve. When these two points are fixed in the coordinate axes, the remaining points can be looked up from this transfer characteristic curve or can be solved from the formula

$$Id = Idss(1- Vgs/Vp)2.$$

- From this formula,we can calculate

  $Vgs = 0, Id = Idss,$

  $Id = 0, Vgs = Vp.$

- The design of JFET is typically designed in the middle between Vp and Idss of the transfer curve .

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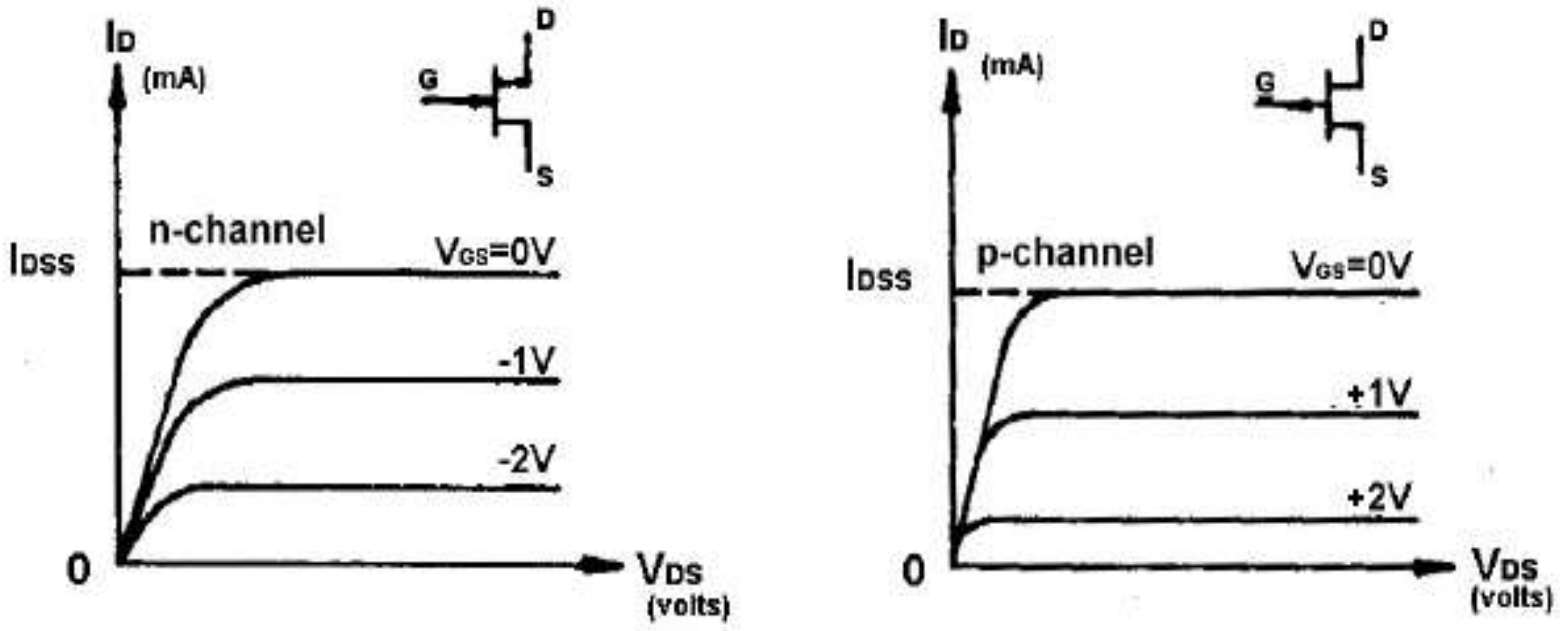
Drain-Source Characteristic Curve



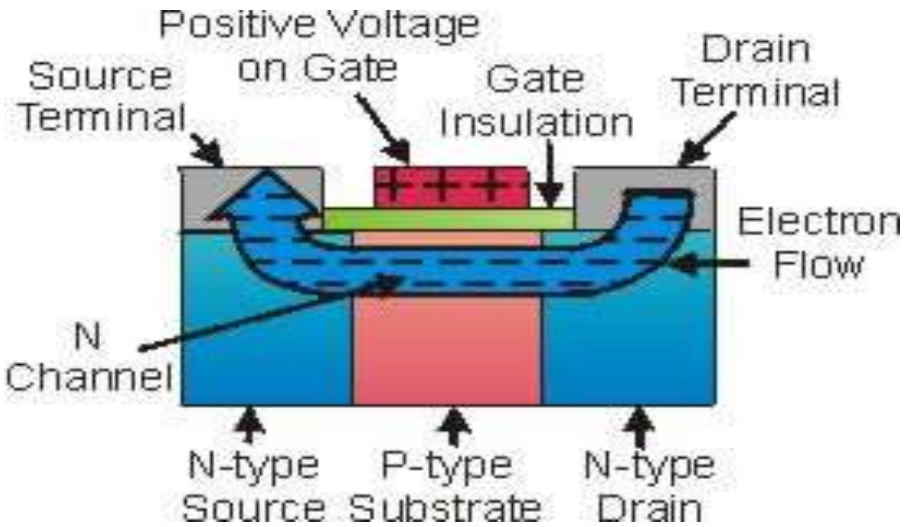
Drain-Source Characteristic Curve of JFET.

- If Vgs is increased (it's more negative to n-channel), depletion will be immediately generated in the channel so that the current required to pinch off the channel will be decreased. The curve corresponding to Vgs = -1V is shown in Fig .
- From this result we can find out that the gate voltage functions as a controller capable of decreasing the drain current (at a specific voltage Vds). If Vgs is more positive for p-channel JFET, the drain current will be decreased from Idss .If Vgs is continuously increased, the drain current will be decreased correspondingly. When Vgs reaches a certain value, the drain current will be decreased to zero and will be independent of the value of Vds.
- The gate-source voltage at this time is called pinch-off voltage which is usually denoted as Vp or Vgs (cutoff). From Fig we can find out that Vp is a negative voltage for n-channel FET and a positive voltage for p-channel FET.

- LECTURE NO. - 45

How a MOSFET Transistor works?

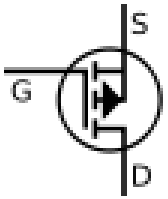
In MosFET, the Gate is insulated from p-channel or n-channel. This prevents gate current from flowing, reducing power usage.

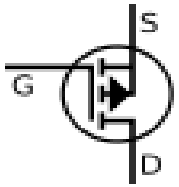


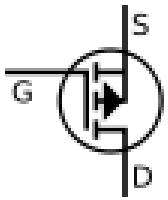
When the Gate is positive voltage ,it allows electrons to flow from drain to source .In this case transistor is on.

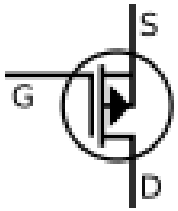
MOSFET

- The **metal–oxide–semiconductor field-effect transistor** (**MOSFET**, **MOS-FET**, or **MOS FET**) is a device used to amplify or switch electronic signals. It is by far the most common field-effect transistor in both digital and analog circuits. The MOSFET is composed of a channel of n-type or p-type semiconductor material (see article on semiconductor devices), and is accordingly called an NMOSFET or a PMOSFET (also commonly nMOSFET, pMOSFET).

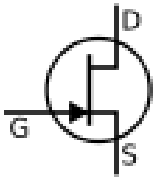


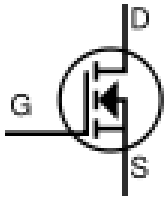


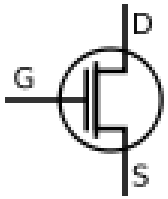


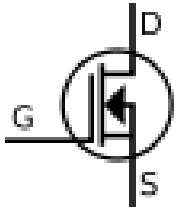


P-channel









N-channel

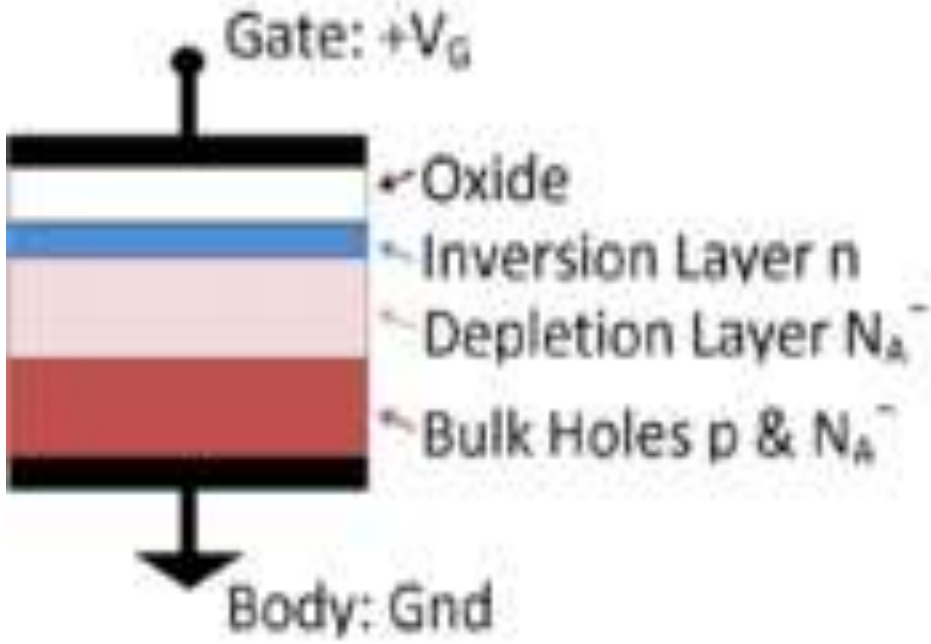
JFET

MOSFET enh

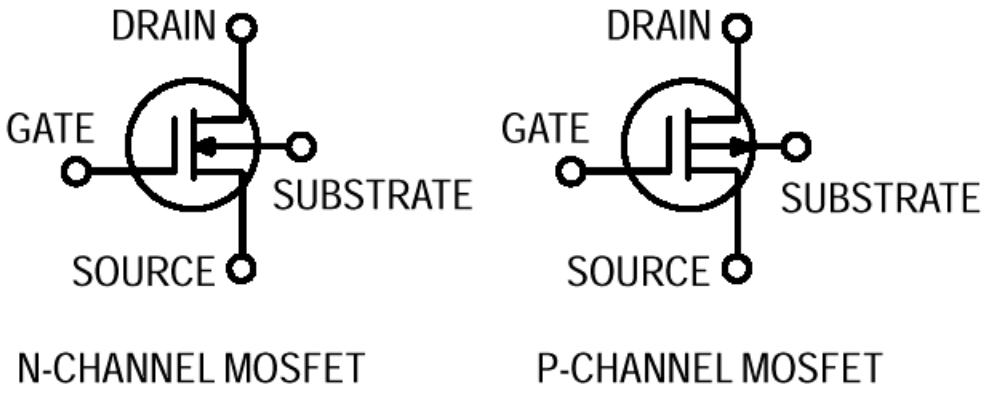
MOSFET dep

MOSFET operation

- **Metal–oxide–semiconductor structure**



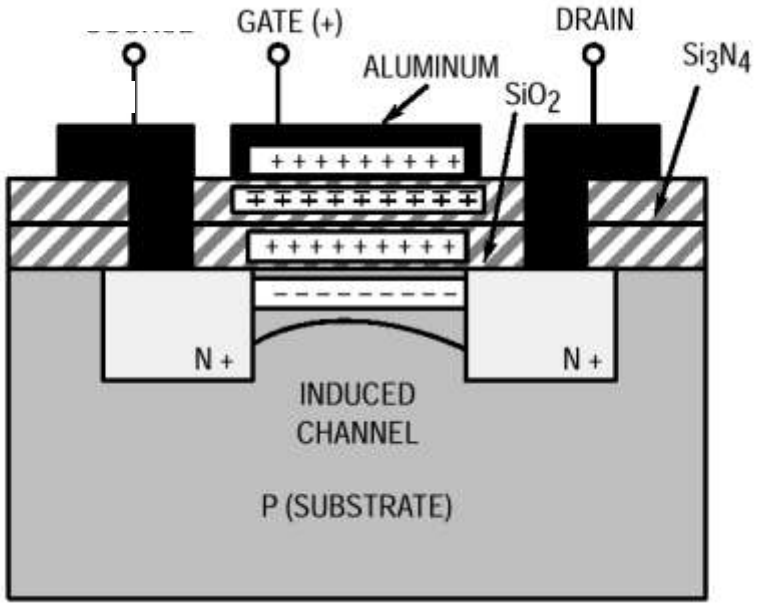
Metal-Oxide-Semiconductor FET



This device is the reason that there are warning labels on almost all computer hardware - “static-sensitive device; handle with care”. Memory in most cases turn out to be MOSFET switches, as is most of the circuitry on the CPU (incidentally the change in operating voltage for the CPU was a result of changing from BJTs to MOSFETs).

As with the JFET there is an additional layer (literally the wafer that it was grown on) that is normally not an external contact - it is internally connected to the source.

Metal-Oxide-Semiconductor FET

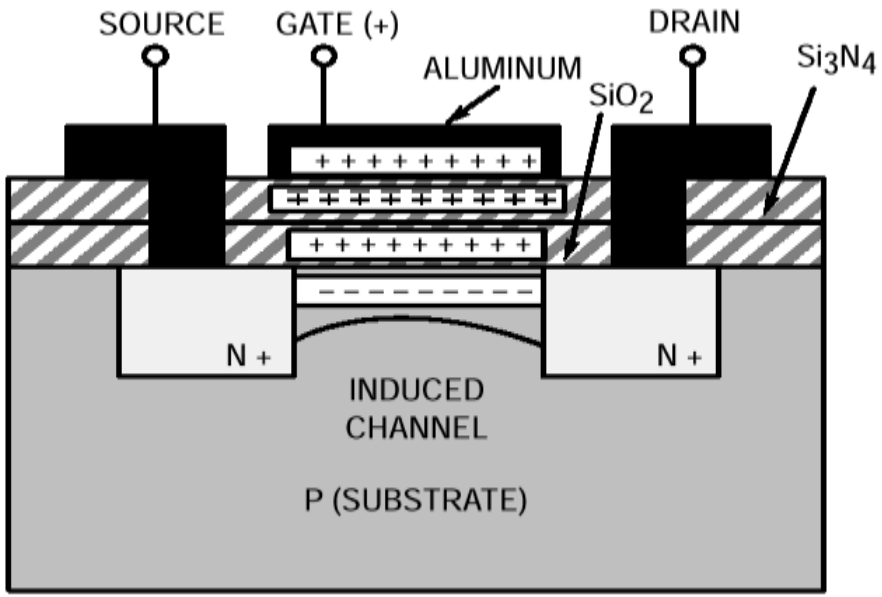


We are only going to talk about the "enhancement" mode, which as the nice feature that as you apply a more and more positive control voltage V_{GS} the current increases. There is also a threshold voltage V_T.

- LECTURE NO. - 46

How does it work? There is no conduction between the source and drain normally (VGS = 0) because regardless of what voltage VDS you apply there is a reverse biased PN junction. Even apply a voltage VGS does not appear from the structure to have an obvious effect since it is not even attached - there is a thin SiO2 insulating layer in between! This gate oxide incidentally is very important - it is one of the current limitations on how fast computers run!

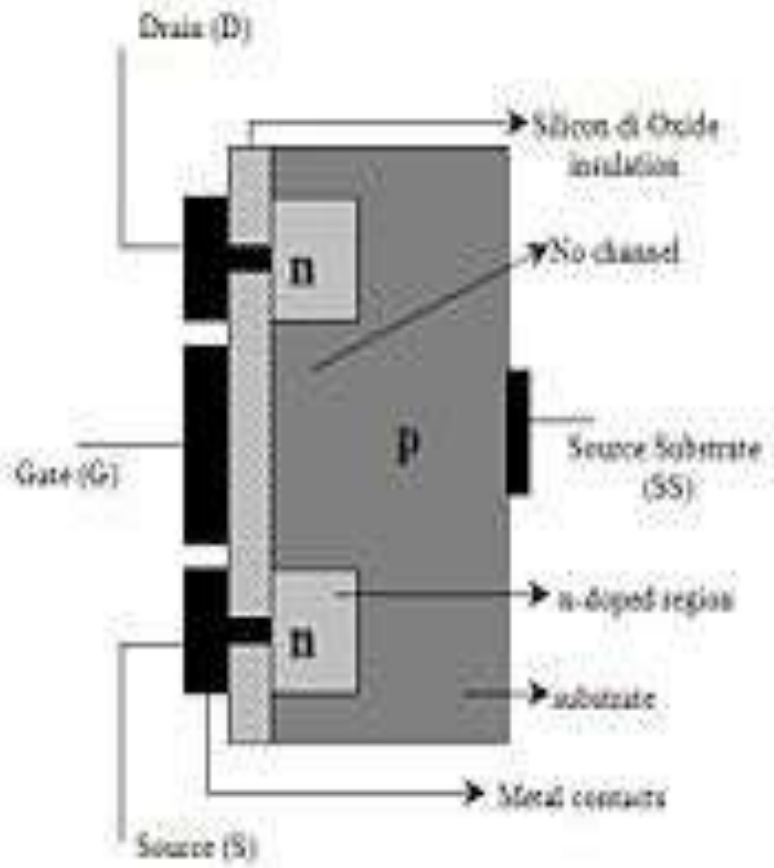
Metal-Oxide-Semiconductor FET(2)



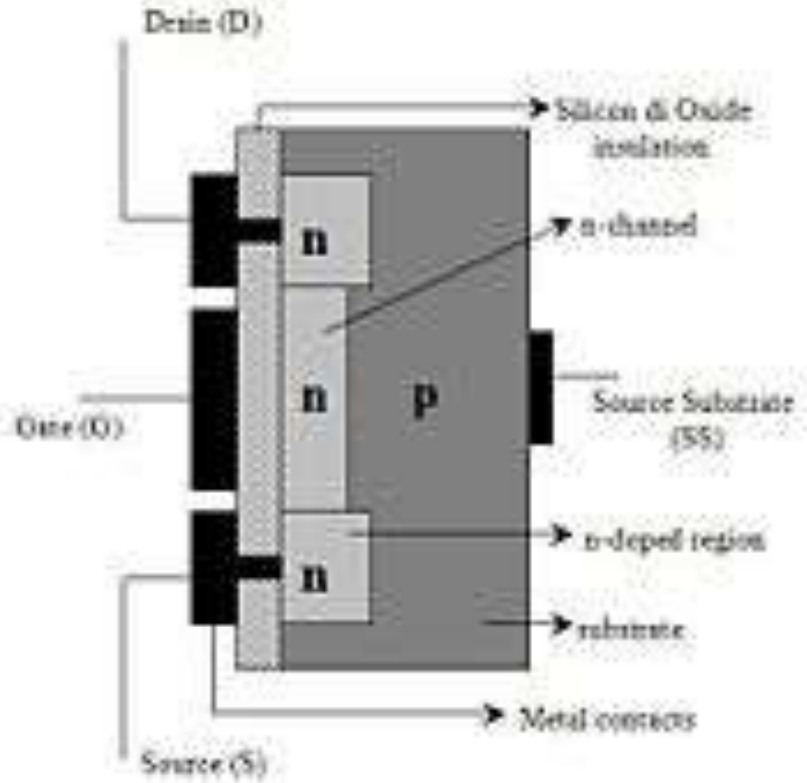
However when you apply a positive voltage the oxide behaves like a capacitor - since positive charge builds up on one side, there must be an equal and opposite charge on the other side.

- This charge must come from the substrate. Since it is P-type there are not many electrons but those that are present are all sucked up to the gate oxide. This creates a region that is very thin, but very rich in electrons, converting P-type to N-type locally. This “channel” is enhanced by applying higher positive biases.
- While there are many applications for MOSFETs (remember they are just like JFETs with the threshold voltage shifted higher) The dominant application is a switch. Most of digital electronics is based on low power switches and most DC power supplies are based on high power switches.

MOSFET structure and channel formation



Cross section of an NMOS without channel formed: OFF state



Cross section of an NMOS with channel formed: ON state

- LECTURE NO. - 47

Modes of operation

- For an **enhancement-mode, n-channel MOSFET** the three operational modes are:
- Cut-off or Sub-threshold or Weak Inversion Mode
- **When *V GS* < *V*th:**
- where *Vth* is the threshold voltage of the device.
- According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source.

- where *ID*0 = current at *VGS* = *Vth* and the slope factor *n* is given by

$$n = 1 + CD / COX,$$

- with *CD* = capacitance of the depletion layer and *COX* = capacitance of the oxide layer. In a long-channel device, there is no drain voltage dependence of the current once *VDS* > > *VT*, but as channel length is reduced drain-induced barrier lowering

Depletion-mode MOSFET

With an appropriate voltage applied between source and drain, current will flow through the channel, as a semiconductor resistance. However, if we now apply a negative voltage to the gate, as shown to the right, it will amount to a small negative static charge on the gate. This negative voltage will repel electrons, with their negative charge, away from the gate. But free electrons are the majority current carriers in the n-type silicon channel. By repelling them away from the gate region, the applied gate voltage creates a depletion region around the gate area, thus restricting the usable width of the channel just as the pn junction did.

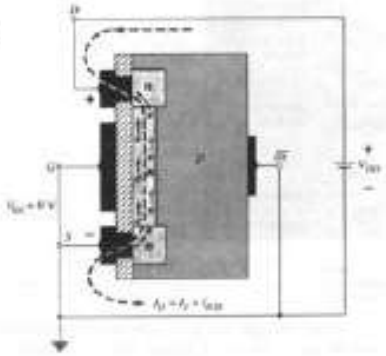
Because this type of FET operates by creating a depletion region within an existing channel, it is called a *depletion-mode MOSFET*.

Depletion type MOSFET-Basic operation

$V_{GS} = 0$ V, $V_{DS} > 0$

Operation similar to JFET

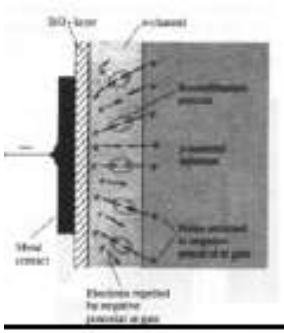
Current flows through *n*-channel. Free electrons are attracted to positive terminal of drain. Channel ohmic resistance is offered.

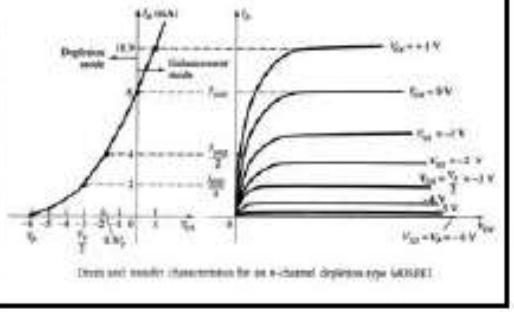


Depletion type MOSFET-Basic operation

When V_{GS} is negative, the electric field will pressure electrons towards *p*-type substrate, hence reduce free carrier in *n*-channel or depleting the majority carrier

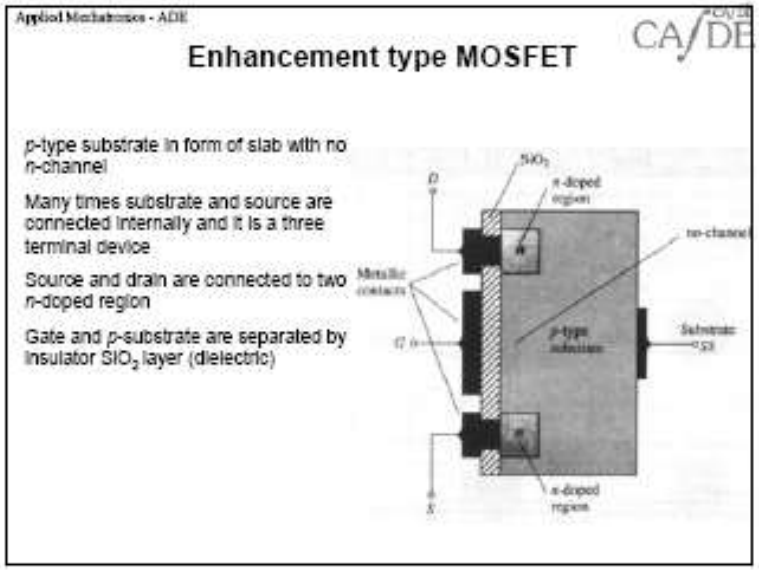
When V_{GS} is positive it enhances the current. It is limited by the maximum current capacity of the device





- LECTURE NO. - 48

Enhancement type MOSFET :



Enhancement type MOSFET

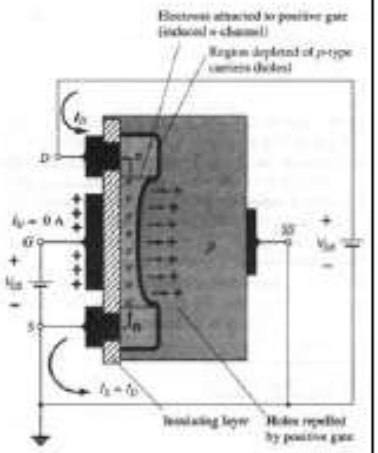
When $V_{GS} = 0$ and $V_{DS} > 0$

No link between two *n*-doped region and hence no current

V_{GS} and $V_{DS} > 0$ This will push the holes away from the SiO_2 edge and attracts electrons from the *p*-substrate. When sufficient voltage is applied it creates a *n*-channel, this is called threshold voltage V_T

If V_{GS} is increased beyond threshold voltage, I_D will increase.

If V_{GS} is kept constant beyond threshold voltage, and V_{DS} is increased then I_D will reach saturation level similar to JFET (pinch off)



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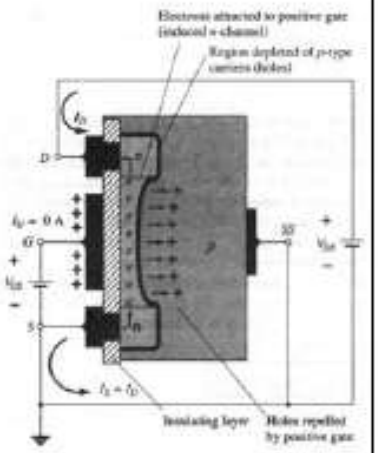
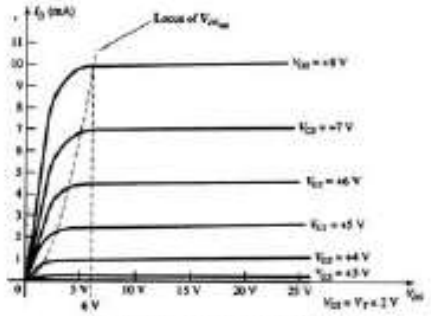


Enhancement type MOSFET

Values less than threshold value I_D is zero

V_{GS} increases V_{DSsat}



Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V^2.

MOSFET amplifiers, have the characteristic of high input impedance. The value of the input impedance for both amplifiers is limited only by the biasing resistors R_{G1} and R_{G2}. Values of R_{G1} and R_{G2} are usually chosen as high as possible to keep the input impedance high. High input impedance is desirable to keep the amplifier from loading the signal source. One popular biasing scheme for the CS and CD configurations consists of the voltage divider R_{G1} and R_{G2}. This voltage divider supplies the MOSFET gate with a constant dc voltage. This is very similar to the BJT biasing arrangement described in Common Emitter amplifier. The main difference with the BJT biasing scheme is that ideally no current flows from the voltage divider into the MOSFET.

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The CS and CD MOSFET amplifiers can be compared to the CE and CC BJT amplifiers respectively. Like the CE amplifier, the CS amplifier has a negative voltage gain and an output impedance approximately equal to the drain resistor (collector resistor for the CE amplifier). The CD amplifier is comparable to the CC amplifier with the characteristics of high input impedance, low output impedance, and less than unity voltage gain. The corner frequencies of the CS and CD frequency response can also be approximated using the short circuit and open circuit time constant methods described in the Common Collector amplifier.

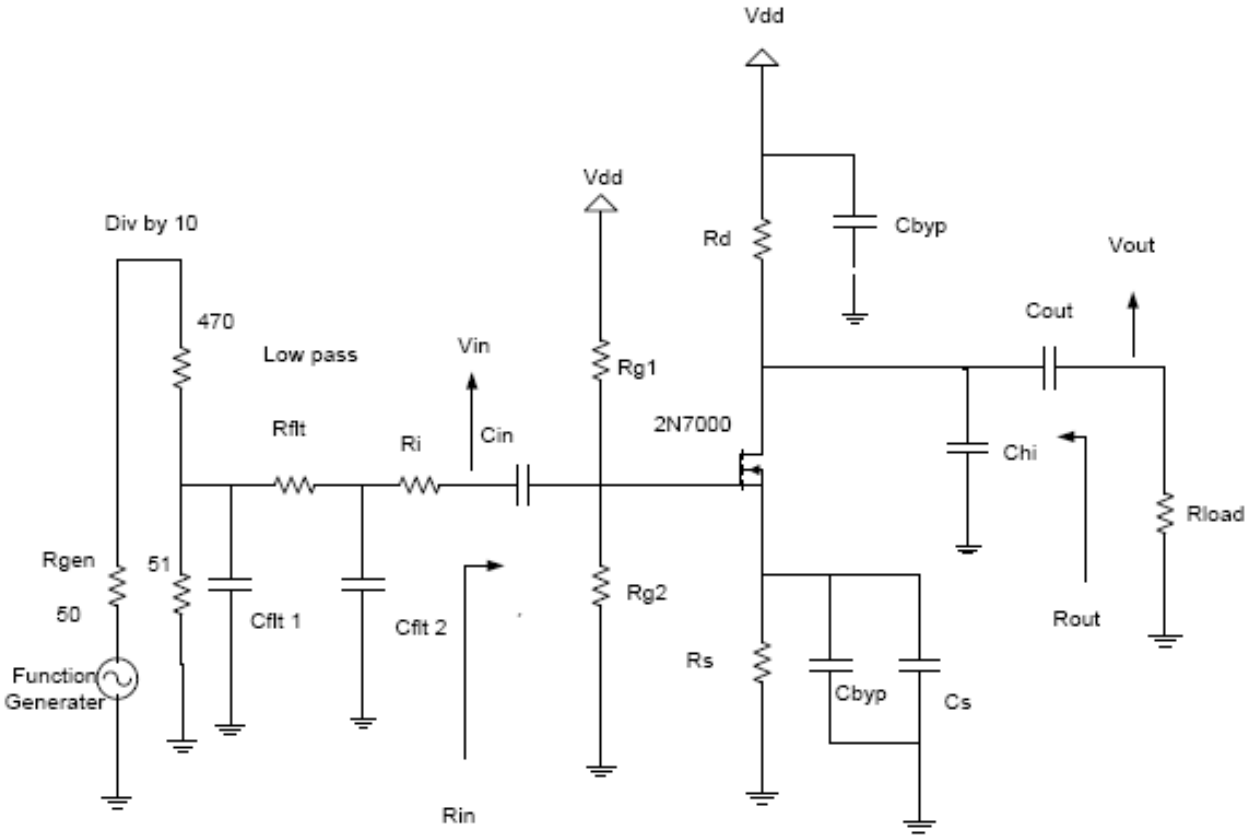


Figure 1: Common Source MOSFET Amplifier

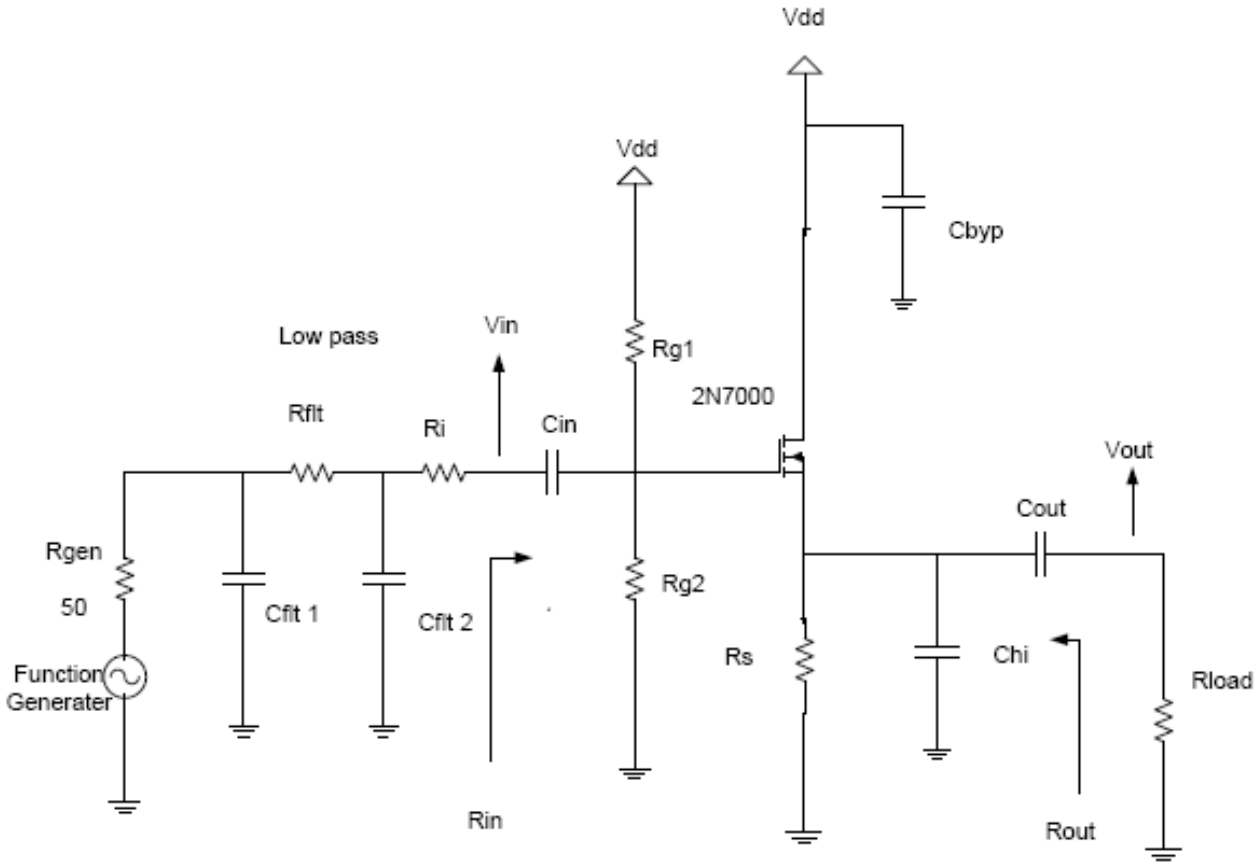
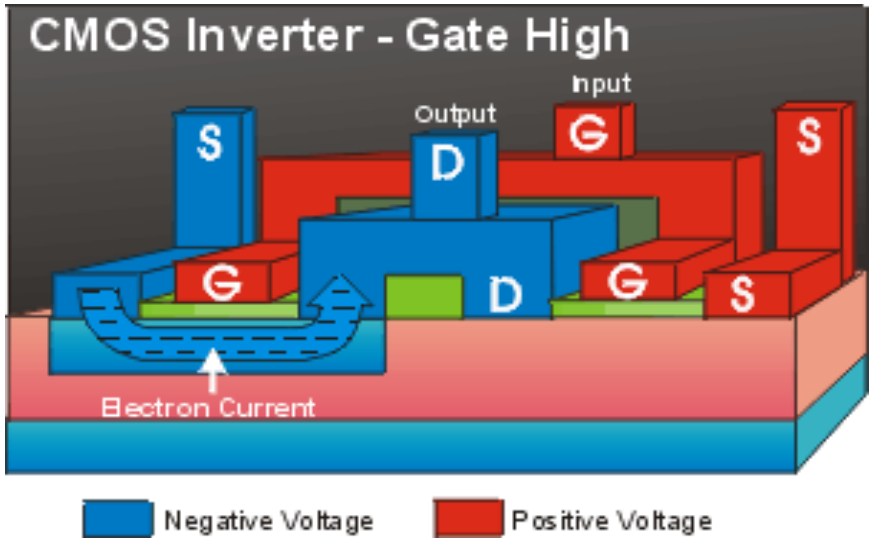


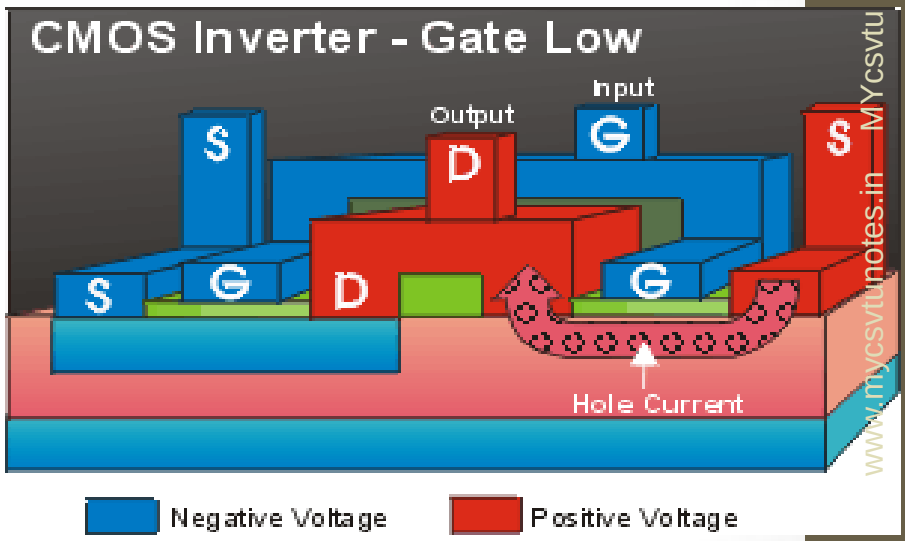
Figure 2: Common Drain MOSFET Amplifier

- LECTURE NO. - 49

How a CMOS transistor works?

N-channel & P-channel MOSFETs can be combined in pairs with a common gate .





When Gate (input) is high ,electrons can flow in N-channel easily . So output becomes low. (opposite of input)

When Gate (input) is low ,holes can flow in P-channel easily. So output becomes high. (opposite of input)

LECTURE NO. - 50

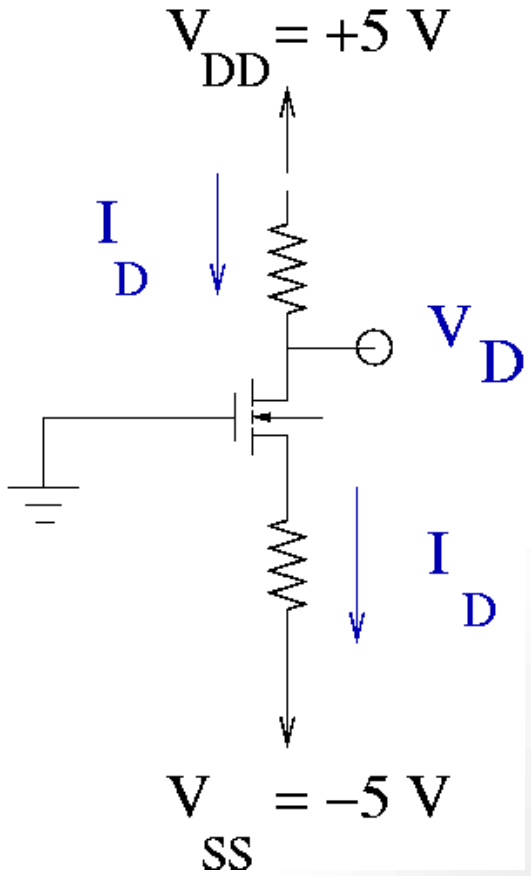
Review of FET operation

- In general, we will use FET in saturation region.

$$0 \geq V_{GS} \geq V_t \geq V_{GD}$$

- Design ckt,

I_D=0.4mA V_D=1V, V_t=2V



$$\mu_n C_{ox} = 20\mu A/V^2, L = 10\mu m, W = 400\mu m$$

Biasing Issues

- V_{GS}=3V, $V_{GS}>V_T$

$$R_S = \frac{V_S - V_{SS}}{I_D}$$

$$R_S = \frac{-3-(-5)}{0.4}$$

$$R_S = 5k\Omega$$

- To establish +1V at drain

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

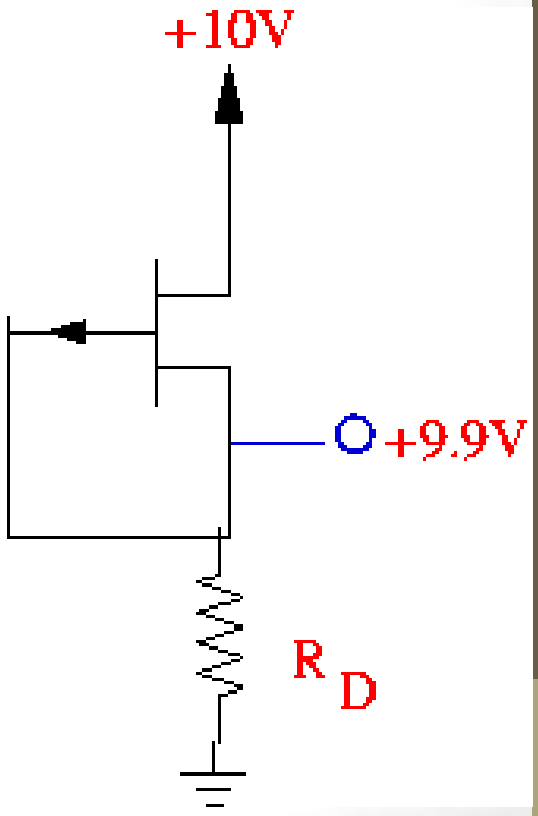
$$R_S = \frac{5-(1)}{0.4}$$

$$R_S = 10k\Omega$$

Biasing (PMOS)

- Design ckt st. +9.9V at the source. Effective resistance r_o ? (Note PMOS)
- V_{GS}=0, V_{GD}=-0.1V < $|V_t|$
- Triode region operation:

$$I_D = 1\left[(0-(-1))x0.1-\frac{1}{2}x0.01\right] \cong 0.1mA$$



Output resistance

- Select:
- Find r_{DS}

$$R_D = \frac{9.9V}{0.1mA} = 99k\Omega \cong 100k\Omega$$

$$r_{DS} = \frac{V_{DS}}{I_D} = \frac{0.1V}{0.1mA} = 1k\Omega$$

Amplifier Circuit

- Input signal v_i
- Output signal v_o

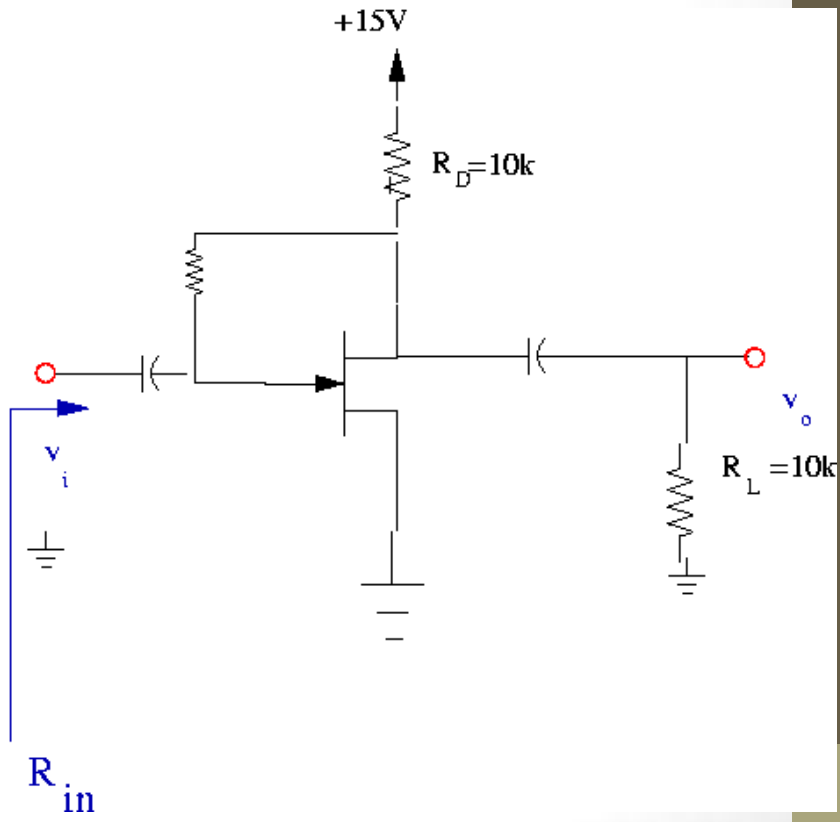
DC bias currents

$$I_D = \frac{1}{2} x 0.25 (V_{GS} - 1.5)^2$$

$$V_D = 15 - R_D I_D = 15 - 10 I_D$$

$$I_D = 1.06 mA$$

$$V_D = 4.4 V$$



Small Signal Parameters

- Find conductance

$$g_m = k'_n \frac{W}{L}(V_{GS} - V_t)$$

$$g_m = 0.25(4.4 - 1.5) = 0.725 mA/V$$

- Output resistance

$$r_o = \frac{V_A}{I_D} = \frac{50}{1.06} = 47 k\Omega$$

Small Signal Gain

- Draw small signal equiv.
- R_G very large > 10M, neglect
- Calculate gain:

$$v_o \cong -g_m v_{gs}(R_D \parallel R_L \parallel r_o)$$

$$\frac{v_o}{v_i} = -g_m(R_D \parallel R_L \parallel r_o) = -3.3$$

- Input resistance:

$$i_1 = (v_i - v_o)/R_G$$

$$i_1 = \frac{v_i}{R_G}[1-(-3.3)] = 4.3\frac{v_i}{R_G}$$

$$R_{in} = R_G / 4.3 = 10M / 4.3 = 2.2M\Omega$$

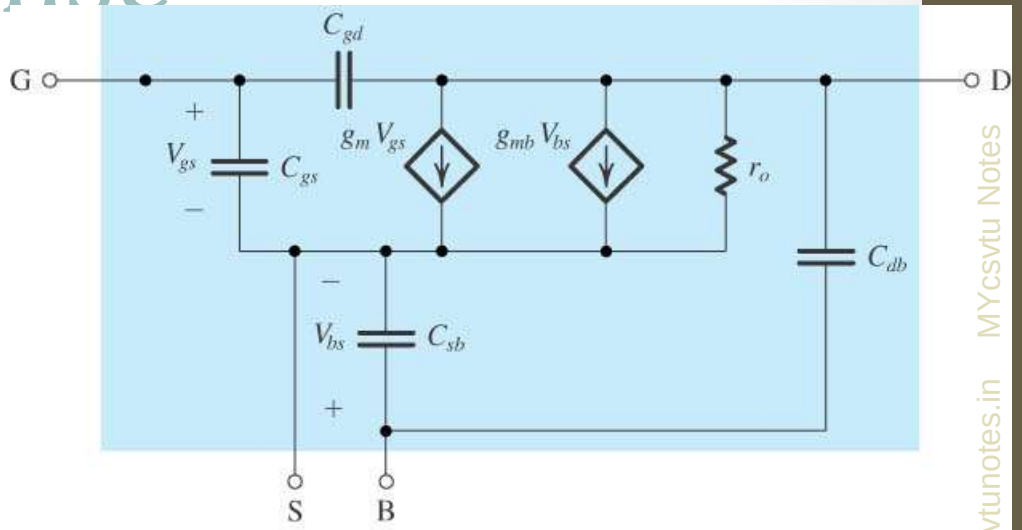
Frequency response

Internal and external capacitances

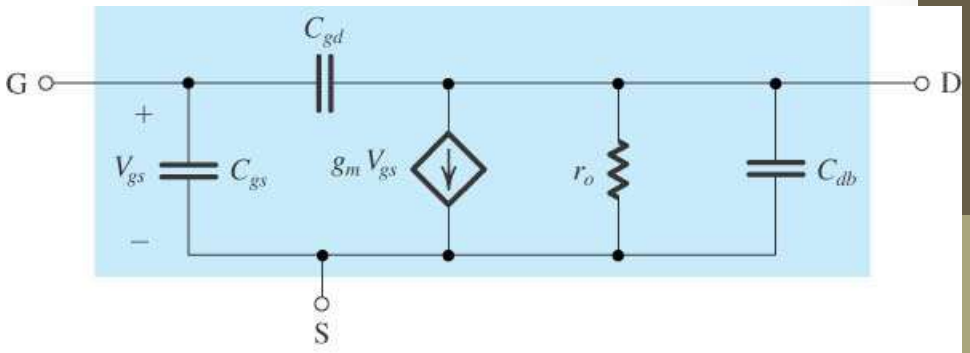
High-frequency equivalent circuit model for the MOSFET (a)

High-frequency equivalent circuit model for the MOSFET when

Source is connected to Body (b)

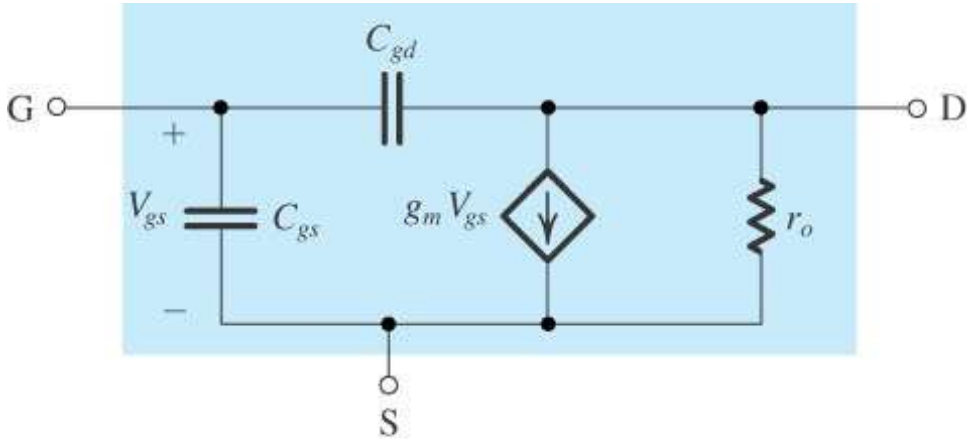


(a)



(b)

Simplified Capacitance Model



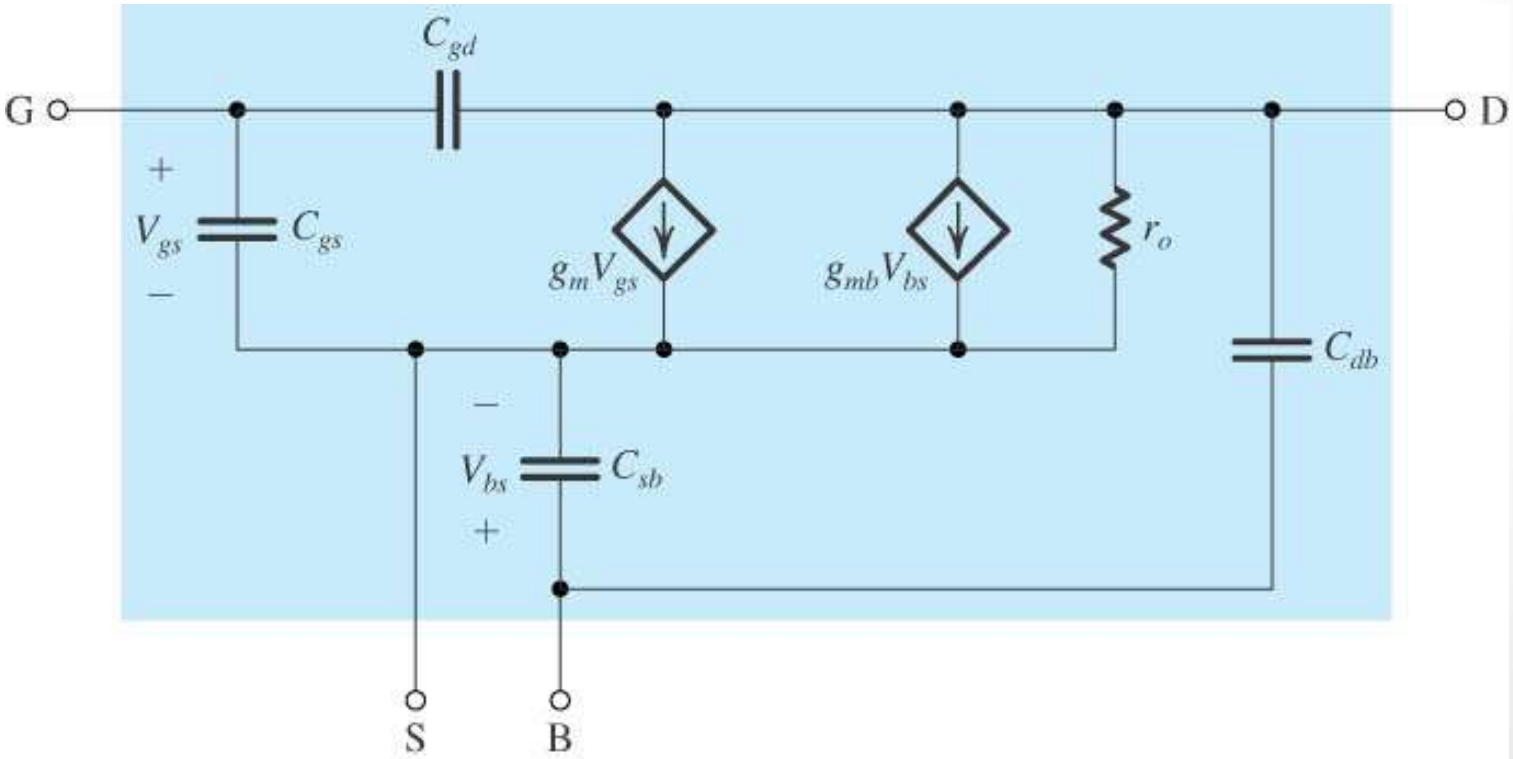
(c)

- Notice we omit capacitance to Body!

MOSFET High Freq. Model

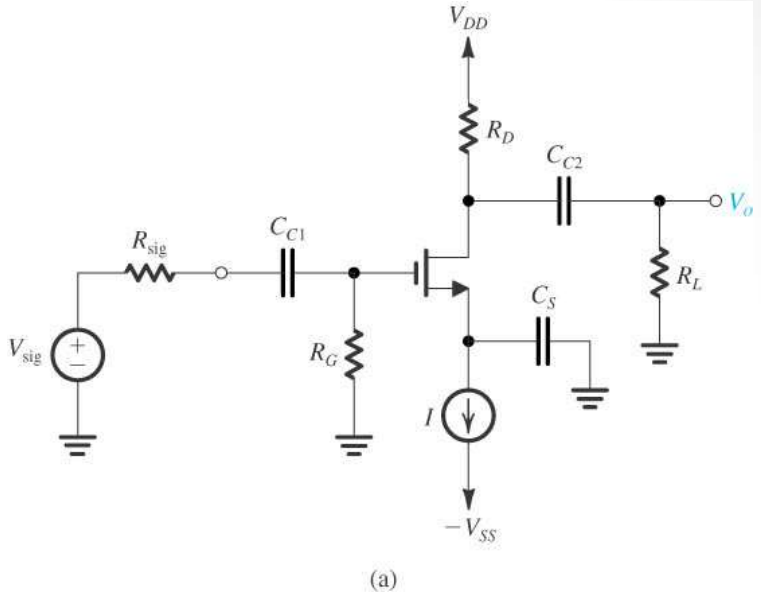
$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = 2\frac{I_D}{V_{OV}}$$

$$C_{gs} = \frac{2}{3} WLC_{ox} + WL_{ov}C_{ox} \qquad C_{gd} = WL_{ov}C_{ox}$$

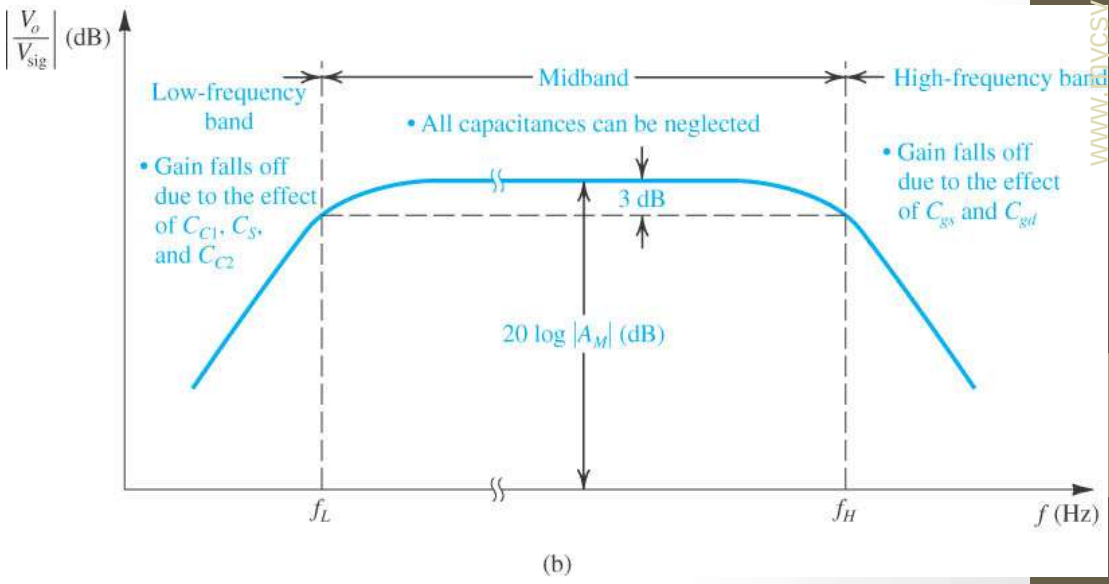


Freq. Response CS

- A_M = ?
- BW=?



(a)



(b)

PROBLEMS