I/O MAPPING

RUNGTA COLLEGE OF ENGG AND TECH.,BHILAI
DEPT OF ELECTRONICS AND TELE. ENGG

I/O mapping

Interfacing I/O devices with MP

• Input device

• Output device

Example: -

When MP wants to read data from input device, the input buffer should enable

Where the signal used to detect the input port

1. $\overline{RD}$ as $\overline{IOR}$

2.   Combinations of address lines

Similarly if Mp wants to write the data on output device, the out put latch should active

Where the signal used to detect the input port

- 1.   WR as IOW

- 2.   Combinations of address lines

Concludes: - Here we can say that I/O devices should have unique address

- Instruction used to input or output data

- ●   IN 8 bit add

- * It is used to input data to accumulator from a port with 8 bit address

-   It is 2 byte instruction and no flags are modified

- * Here the 8 bit address is transferred to $A_0 - A_7$ and same as to access the data from

-   port $A_8 - A_{15}$

Example : - IN 20H

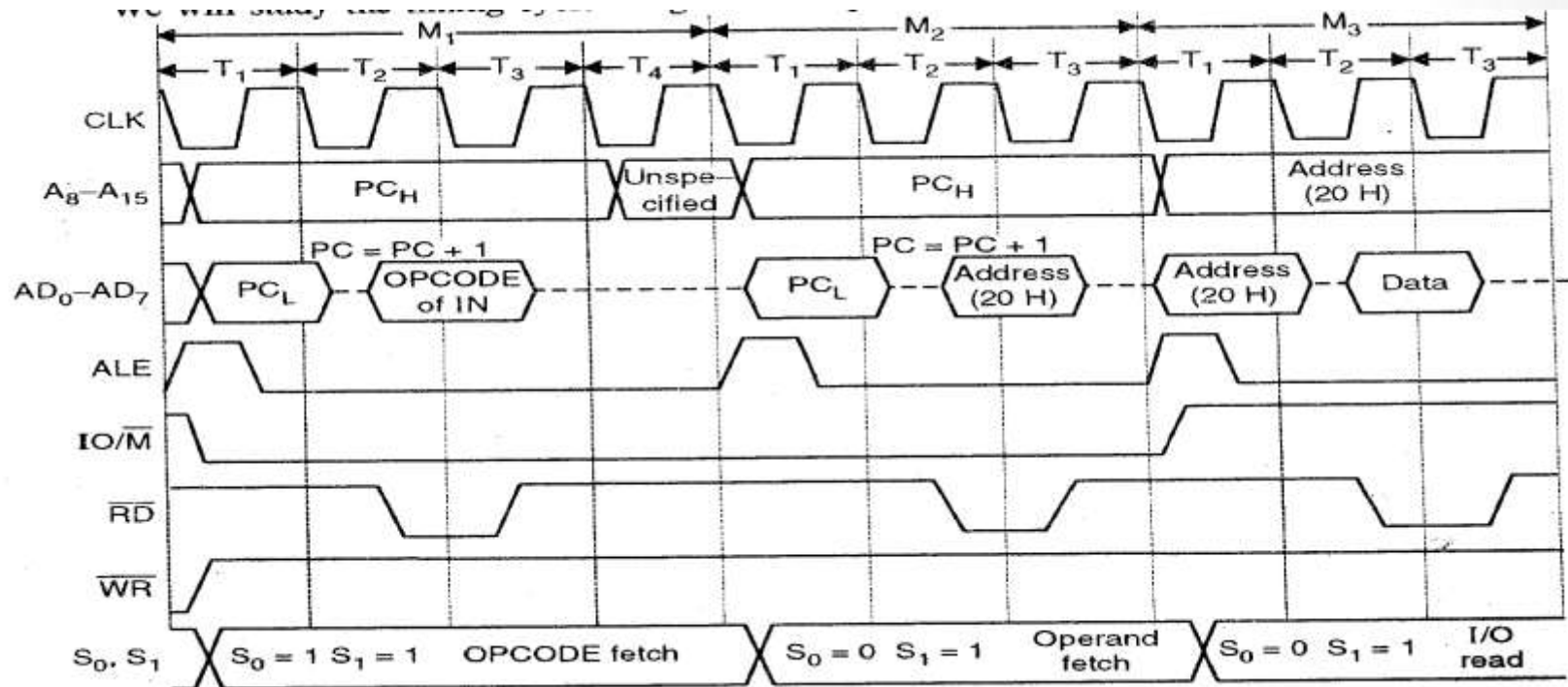Timing Diagram of instruction IN 20H

Fig. 9.3 : Timing diagram of IN 20

NOTE : - Since the I/O address is 8 bit so the range of I/O address is from 00 H to FF H

Hence total 256 address may possible for I/O mapping

- Q.1 What is the status of $A_8 - A_{15}$ while the 3rd T state of In instruction

- Ans We have 16 bit of address line in 8085 but in I/O mapping the specified address is of 8 bit so to implement this 8 bit address is transferred on both address group

- Out 8 bit add

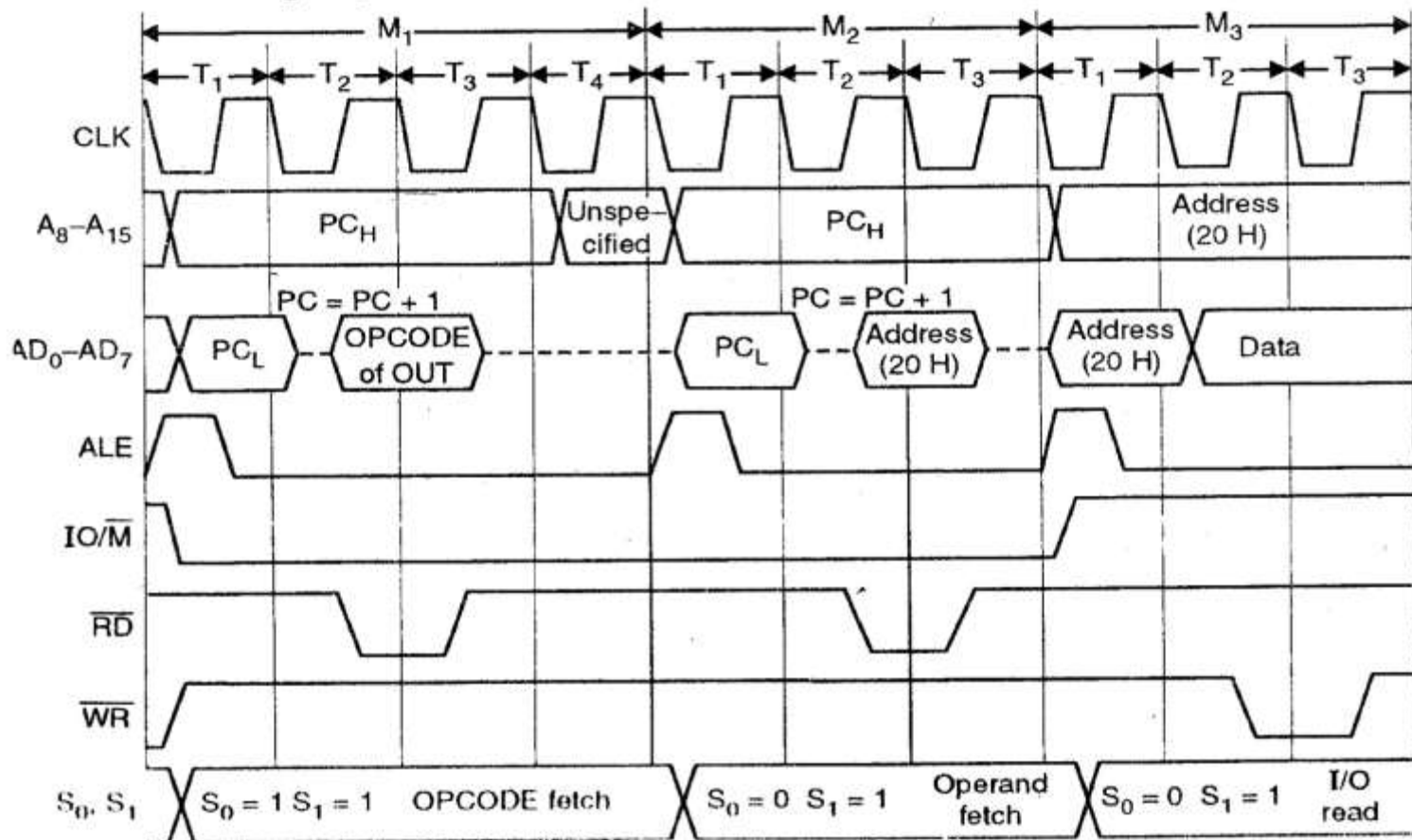* It is used to send the data for accumulator to output port

  It is 2 byte instruction and no flags are modified

* Here the 8 bit address is transferred to $A_0 - A_7$ and same as to access the data from

  port $A_8 - A_{15}$

Timing diagram of OUT 20H

In 3rd T state the address lines are loaded by specified address

I/O mapped I/O

In I/O mapped I/O we have to specific add for I/O device this address are provided by Decoder logic

 Example- Interface Input buffer with input address FF H

And out put latch with address FE H

Step III : Interfacing buffer,

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Device address
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	
1	1	1	1	1	1	1	1	FF H

Output from decoder logic, required is **"LOW"**.

∴ Use NAND gate. Presently, we will consider all the address lines, i.e. absolute decoding. The diagram is shown in Fig. 9.5.
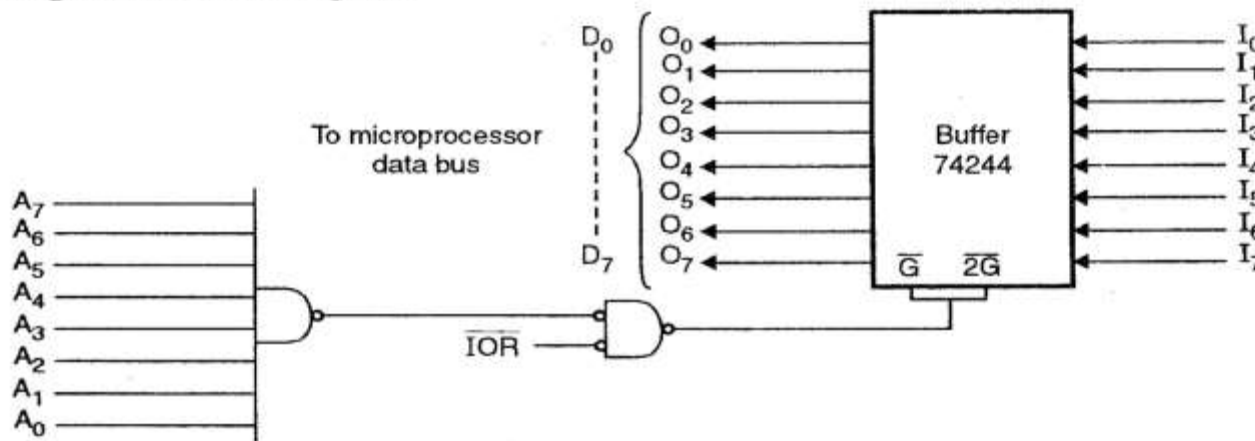

Fig. 9.5 : Input port interfacing in IO mapped I/O

Step IV : Interface latch,

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Device
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	address
1	1	1	1	1	1	1	0	FE H

Note : For latch, to be enabled, we require HIGH logic, not LOW logic.

So again we will use 8 input NAND, with two input AND. The interfacing is shown in Fig. 9.6.
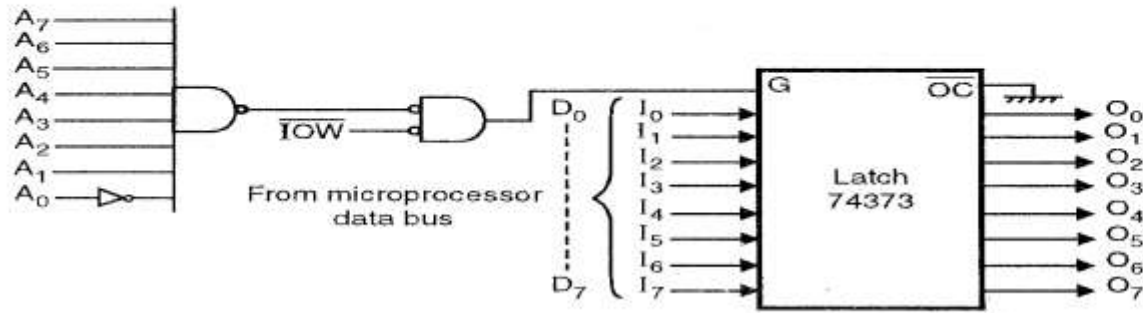

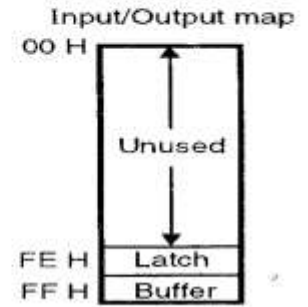**Fig. 9.6 : Output port interfacing in IO mapped I/O**

Fig. 9.7

Points :

(1)   We can map I/O device, any where in I/O map.

(2)   It is not essential to use, all the addresses. Few can be unused, depending upon application
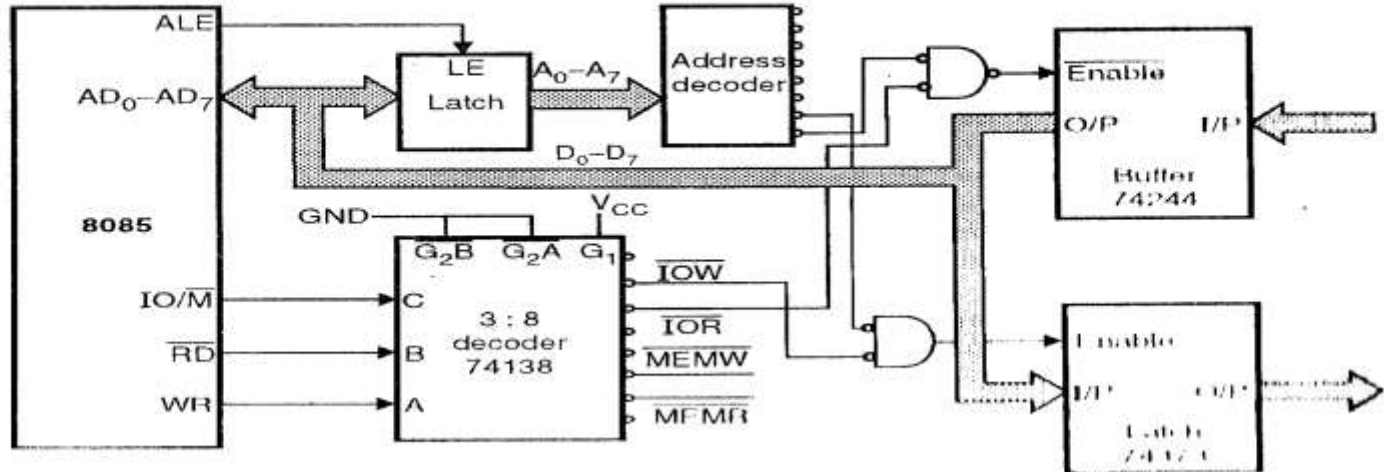   We can now draw a generalised block diagram for I/O device interfacing. Refer Fig. 9.8.

Fig. 9.8 : General I/O device interfacing

Example 2

Interface 8 LED to 8085 using buffer and latch as a input and out put device and also write a program to take data from to take switched data from input buffer and display it on LED

Input address is   FF H

Output address is FE H

Connect switch with buffer and Led with latch

Input logic   0   switch is pressed

              1   other wise
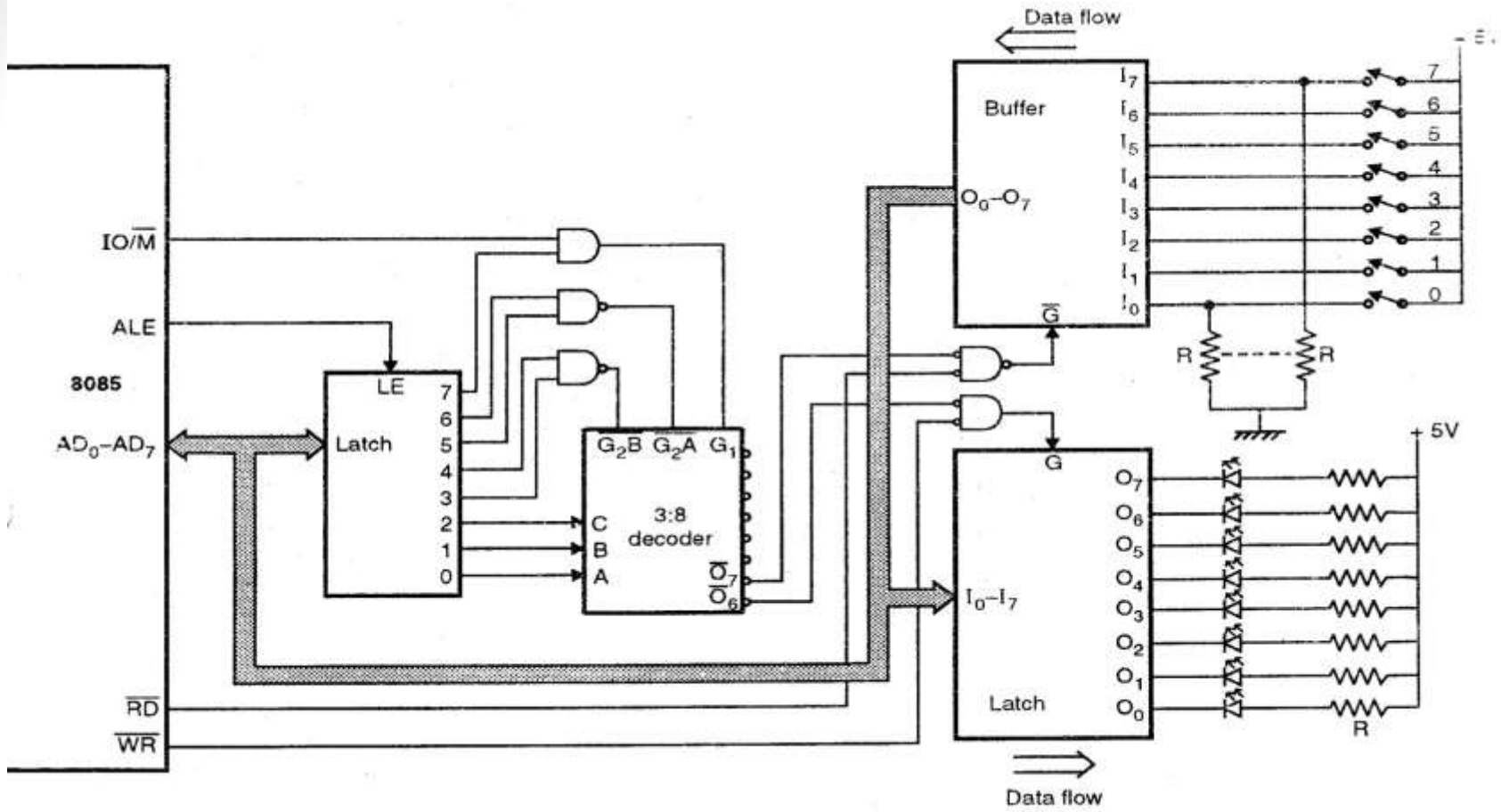
output logic 0   LED glow

              1   Led off

Fig. 9.12 Buffer and latch interfacing in I/O mapped I/O.

Instead of using lower order address line one can use higher order address line so that demultiplexing of lower order address and data line may be neglected

Program: -

    up IN FF H

        CMA

        Out FEH

        JMP up

        HLT

Shadowing Effect

While designing decoder logic for I/O mapped if the number of I/O devices are less we can use linear or partial decoding

Here we consider some of the address line as Do't care Due to this instead of providing specific address we get multiple address

Memory Mapped I/O

In memory mapped I/O technique I/O device can be treated as memory location

There is no separate add and I/O address

I/O address is not 256 here but whole 64 kb memory is shared by I/O and memory

Step II :

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Device address
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	I/P (FFFF H)
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	O/P (7FFF H)

Presently we will use simple logic gates to design decoder logic. One can also use 3:8 decoder (74138).
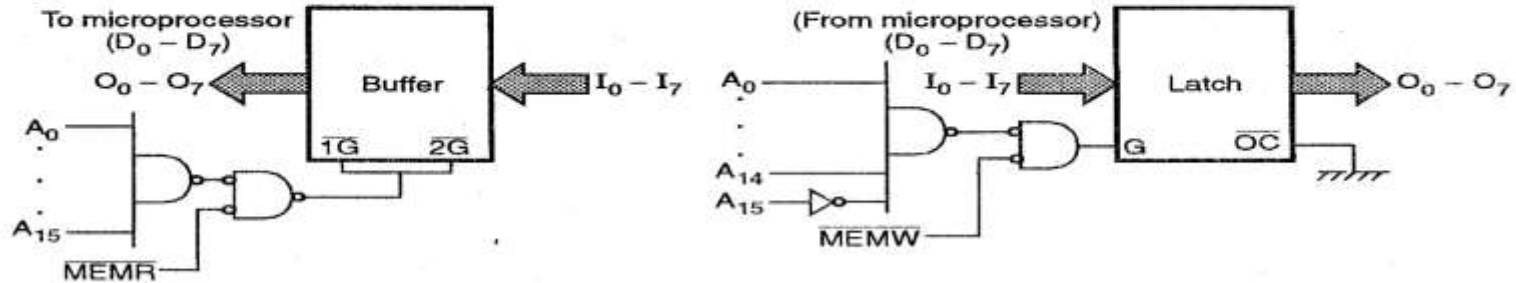
Step III : Interfacing diagram

Fig. 9.16 : I/O interfacing in memory mapped I/O

The combination of address lines A_0 to A_{15} can be done by using NAND gates and then it is combined with $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$ signal. The interfacing diagram will be as shown in Fig. 9.16.

For buffer when A_0 to A_{15} all are 1's the output of NAND gate will be low. It is then combined with $\overline{\text{MEMR}}$ using NAND gate with inverted inputs and connected to $\overline{1G}$ and $\overline{2G}$. So the address of buffer will be FFFF H. For latch when A_0 to A_{14} all are 1's and the line $A_{15} = 0$ the output of NAND gate will be LOW, it is then combined with $\overline{\text{MEMW}}$ using AND gate with inverted inputs and connected to G, So the address of latch will be 7FFF H.

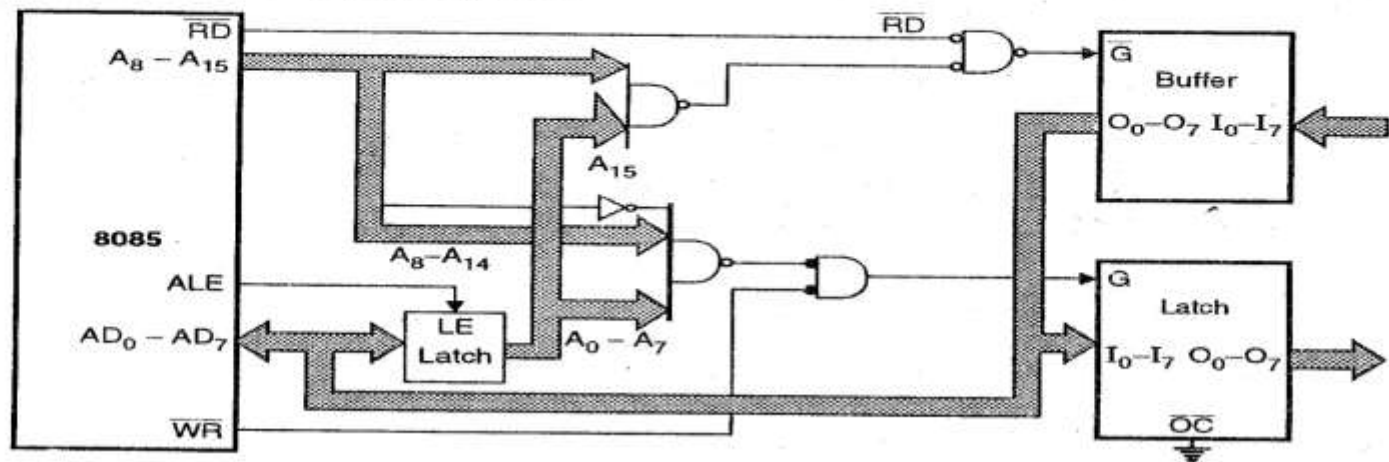**Step IV :** The general interfacing diagram of an I/O device with 8085 in memory mapped I/O scheme is as shown in Fig. 9.17.

Fig. 9.17 : I/O interfacing in memory mapped I/O