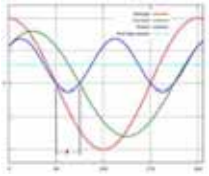
POWER ELECTRONICS


NOTES

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05B-001-EE SEC:A

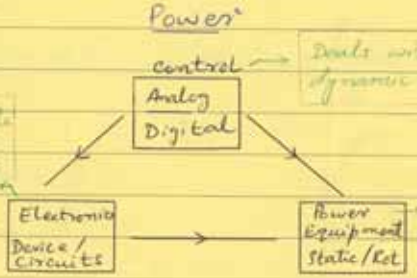
Date 06-02-2008

Power Electronics :

(Combination of Power, Control & Electronics)

Defn:

"The applications of solid state electronics for the control & conversion of electrical power."



Application:

- Heat Controls
- Light Controls
- Motor Controls
- Power Supplies.
- Vehicle Propulsion Systems
- High Voltage Direct Current (HVDC)

Skin Effect: There is no skin effect w.r.t D.C

- Skin effect based on the frequency of A.C. w/e causes $X_c \neq X_L$ (Loses)

In a conductor carrying an alternating current, an electromagnetic effect which results in current density being greater at surface of conductor than in centre at sufficiently high frequencies current is practically confined to surface of conductor.

AC to DC Conversion

Date 07-02-2009

UNCONTROLLED RECTIFICATION

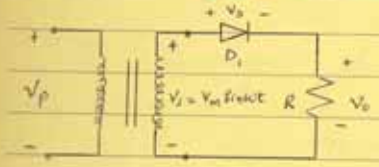
Rectifier: Converts AC to DC.

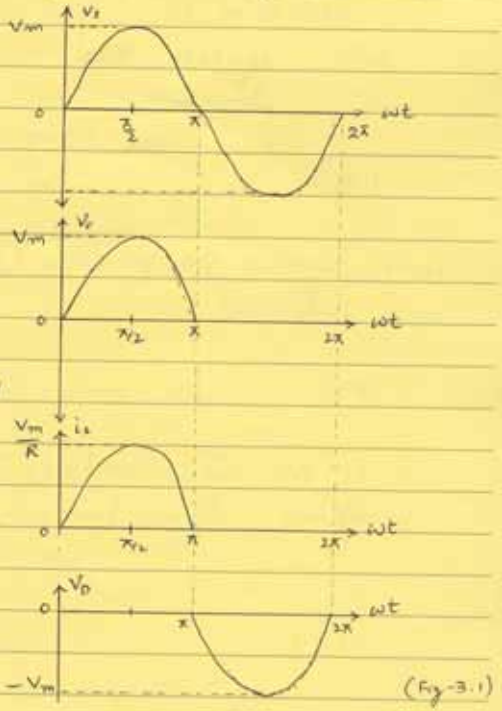
Depending upon i/p supply there are two types of rectification:

(i) Single Phase (ii) Three Phase

{For simplification in analysis considering diodes to be lossless or ideal - meaning no Forward voltage drop}

SINGLE PHASE HALF-WAVE RECTIFIER





(Fig-3.1)

- A Single Phase halfwave rectifier is the simplest power electronics based circuit that is used only rare for low cost power supplies that are used in radios.

- The o/p is discontinous and contain harmonics we expect from rectifier To have constant dc o/p with minimal harmonics

- For i/p side it must have a high power (ideally units) that means i/p current and voltage must be in Phase.

Date 07-02-08

- Discontinous nature of wave ⇒ Harmonic Distortion.
- As # of harmonics increases its strength decreases. Harmonics are the integral multiple of fundamental.

PERFORMANCE PARAMETERS:

- Power factor is defined as $P = VI$ (DC)
  $P = VI \cos\phi$ (AC)
- The average value of o/p load voltage, V_{dc}
- " " " " current, I_{dc}
- Output dc Power is given as:

$$P_{dc} = V_{dc} \cdot I_{dc} \quad (3.1)$$

- The root-mean-square (rms) value of o/p voltage, V_{rms}
- " " " " current, I_{rms}
- Output ac Power is:

$$P_{ac} = V_{rms} \cdot I_{rms} \quad (3.2)$$

- The η (efficiency) or rectification ratio, w/c is a figure of merit and permit us to compare effectiveness, is defined as

$$\eta = \frac{P_{dc}}{P_{ac}} \quad (3.3)$$

- The o/p voltage can be considered as compound of two components:
  (1) The DC value
  (2) The AC component or ripple.

Date 07-02-2008

- The effective rms value of the ac component of o/p voltage is

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2} \qquad (3.4)$$

- The form factor, which is measure of shape of output voltage is

$$FF = \frac{V_{rms}}{V_{dc}} \qquad (3.5)$$

- The ripple factor, w/c is measure of ripple content, is defined as

$$RF = \frac{V_{ac}}{V_{dc}} \qquad (3.6)$$

Substituting Eq (3.4) in (3.6) the ripple factor can be expressed as

$$RF = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{FF^2 - 1} \qquad (3.7)$$

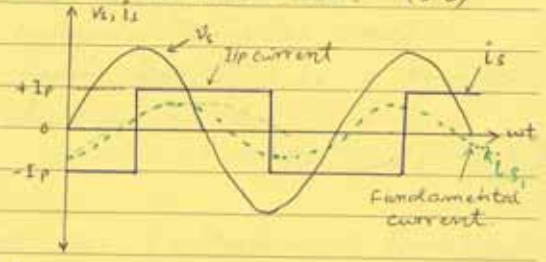
- The transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{V_s I_s} \qquad (3.8)$$

* Reflected is not written due to resistive load.

where V_s & I_s are the rms voltage and current of txfr secondary respectively.

Let us consider waveform of fig 3.2 where v_s is sinusoidal i/p voltage and i_s is the sinusoidal i/p current and i_{s_1} is its fundamental component.



(Fig 3.2)

Date 07-02-2008

- If ϕ is angle b/w fundamental components of i/p current and voltage, ϕ is called Displacement factor (angle) and defined as

$$DF = \cos\phi \qquad (3.9)$$

- The Harmonic factor of input current is given as.

$$HF = \left(\frac{I_s^2 - I_{s_1}^2}{I_{s_1}^2}\right)^{1/2} = \left[\left(\frac{I_s}{I_{s_1}}\right) - 1\right]^{1/2} \qquad (3.10)$$

where I_{s_1} is fundamental comp. of i/p current I_s. Both I_s and I_{s_1} are rms here.

- The input Power factor is defined as

$$PF = \frac{V_s I_{s_1}}{V_s I_s} \cos\phi = \frac{I_{s_1}}{I_s} \cos\phi \qquad (3.11)$$

- The Crest factor w/c is measure of Peak i/p current $I_{s(peak)}$ as compared with its rms value I_s, is often of interest to specify peak current rating of devices and components. CF of i/p current is defined as.

$$CF = \frac{I_{s(Peak)}}{I_s} \qquad (3.12)$$

NOTES:

(1) HF is measure of distortion of a waveform and is also known as Total Harmonic Distortion (THD).

(2) If i/p current i_s is purely Sine. $I_{s_1} = I_s$ & PF = DF. The ϕ becomes impedance angle

$$\Theta = \tan^{-1}(\omega L/R)$$

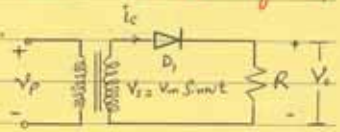
for RL load.

(3) DF is often known as Displacement Power factor. (DPF)

(4) An ideal rectifier should have $\eta = 100\%$, $V_{ac} = 0$ RF = 0, TUF = 1, HF = THD = 0, PF = DPF = 1.

(Example 3.1) Date 07-02-08

Question No.1: Find performance parameter of Half wave rectifier. The rectifier in fig 3.1 a has a purely resistive load of resistor (R). Determine (a) Efficiency (b) FF (c) RF (d) TUF (e) PIV of D_1 (f) CF of I/p Current (g) I/p PF.



Solution:

The average o/p voltage V_{dc} is defined as,

$$V_{dc} = \frac{1}{T}\int_0^T V_L(t)\,dt$$

We can notic from fig no. 3.1 (b), the $V_L(t) = 0$ for $T/2 \le t \le T$, Hence we have

$$V_{dc} = \frac{1}{T}\int_0^{T/2} V_m \sin\omega t\,dt$$

$$= \frac{V_m}{T}\left|\frac{-\cos\omega t}{\omega}\right|_0^{T/2}$$

$$= -\frac{V_m}{\omega T}\left\{\cos\frac{\omega T}{2} - \cos 0\right\}$$

$$= -\frac{V_m}{\omega T}\left\{\cos\frac{\omega T}{2} - 1\right\}$$

$V_{dc} = \frac{-V_m}{2\pi \times \frac{1}{f}}\left\{\cos 2\pi f \times \frac{1}{2f} - 1\right\}$

$V_{dc} = \frac{-V_m}{2\pi}(-2) = \frac{V_m}{\pi}$

However freq of source is $f = \frac{1}{T}$ & $\omega = 2\pi f$

Thus; $V_{dc} = \frac{V_m}{\pi} = 0.318\,V_m$

$$I_{dc} = \frac{V_{dc}}{R} = \frac{0.318\,V_m}{R}$$

The rms value of periodic waveform is defined as

$$V_{rms} = \left[\frac{1}{T}\int_0^T V_L^2(t)\,dt\right]^{1/2}$$

Date

$$V_{rms} = \left[\frac{1}{T}\int_0^{T/2} (V_m \sin\omega t)^2\,dt\right]^{1/2}$$

$$= \frac{V_m}{2} = 0.5\,V_m$$

$$I_{rms} = \frac{V_{rms}}{R} = \frac{0.5\,V_m}{R}$$

(a)

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(0.318\,V_m)\left(\frac{0.318\,V_m}{R}\right)}{(0.5\,V_m)\left(\frac{0.5\,V_m}{R}\right)}$$

$$= 0.4044 \times 100$$

$$\eta = 40.44\,\%$$

(b) $$FF = \frac{V_{rms}}{V_{dc}}$$

$$= \frac{0.5\,V_m}{0.318\,V_m}$$

$$= 1.572 \quad \text{or} \quad 157.2\,\%$$

(c) $$RF = \frac{V_{ac}}{V_{dc}}$$

$$RF = \sqrt{FF^2 - 1}$$

$$RF = \sqrt{(1.57)^2 - 1} = 1.21 \text{ or } 121\,\%$$

(d) TUF

$$V_s = \frac{V_m}{\sqrt{2}} = 0.707\,V_m$$

$$TUF = \frac{P_{dc}}{V_s I_s}$$

Q no: 3.1 Date 13-02-2008

$$I_s = \frac{0.5 V_m}{R}$$

Now $TUF = \dfrac{0.318 V_m \times 0.318 \frac{V_m}{R}}{0.707 V_m \times 0.5 \frac{V_m}{R}}$

$TUF = 0.286$

(f)

$PIV = V_m$ $\qquad \frac{1}{TUF} = 3.496$

$I_{s(peak)} = \frac{V_m}{R}$, $I_s = 0.5 \frac{V_m}{R}$

$$CF = \frac{I_{s(Peak)}}{I_s}$$

$$CF = \frac{1}{0.5} = 2$$

(g) $I/P\ PF = \dfrac{P_{ac}}{V.A} = \dfrac{(0.5)^2}{0.707 \times 0.5} = 0.707$

Note: $1/TUF = 3.496$ signifies that txfr must be 3.496 times larger that when it is used to deliver power from a pure ac voltage. This rectifier has ripple factor of 121%; a low efficiency 40.5% and poor TUF 0.286
In addition txfr has to carry a dc current and this result in a dc saturation problem of transformer core.

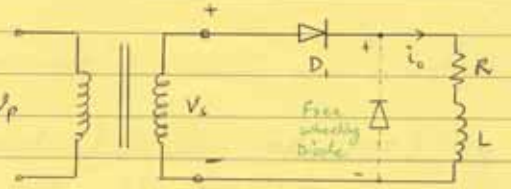
* TUF → How lossy is system? more loses less the TUF. (Transformer Utilization Factor).

Date 13-02-2008

Core Saturation:

Single Phase Half Wave Rectifier With RL Load

* Due to inductive load conduction period of diode will extend beyond 180° until current becomes zero at $\omega t = \pi + \delta$



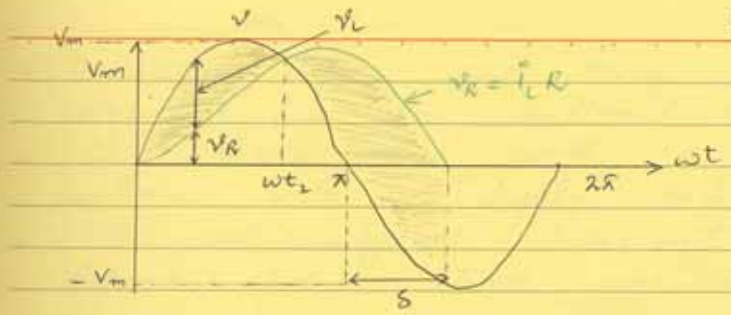
* The average o/p voltage is given by:

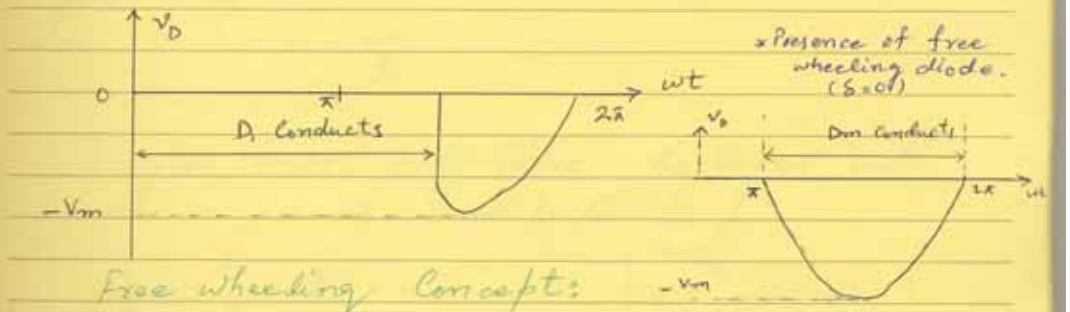
$$V_{dc} = \frac{V_m}{2\pi} \int_0^{\pi+\delta} \sin\omega t \, d(\omega t) = \frac{V_m}{2\pi} \left[-\cos\omega t\right]_0^{\pi+\delta}$$

$$V_{dc} = \frac{V_m}{2\pi} \left[1 - \cos(\pi+\delta)\right]$$

$$I_{dc} = \frac{V_{dc}}{R}$$

Date 13-02-2008





* Presence of free wheeling diode. ($\delta = 0$)

Free wheeling Concept:

* The average V and I can be inc↑ by making $\delta = 0$ w/c is possible by adding FREE WHEELING Diode(s).

* The fns of diode is that restricts -ve voltage developing across load. This inc↑ magnets stored energy of inductor.

* At $t_1 = \pi/\omega$ current is transferred from D_1 to D_m & process is called diode commutation. The waveforms are:

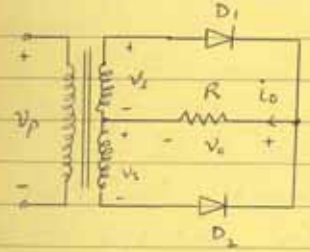
* If 'L' value is inc↑ so that waveform will be comes continous

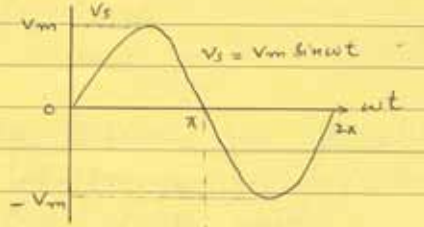
Date 14-02-2008

* Depending upon load time constant current can be continous or discontinous.
* Its discontinous with a R-load & continous with a highly inductive load.
* The continuity of current would depend upon time constant w/c is given by

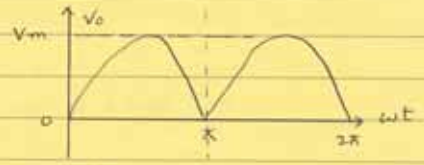
$$\tau = \frac{\omega L}{R}$$

Single Phase Full-wave Rectifier with a Resistive load



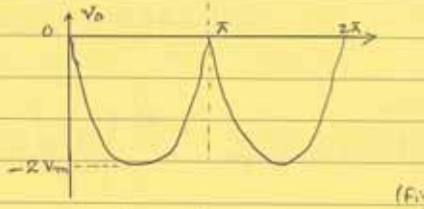


(x) In this design PIV rating of diode is to be chosen high limit or rating.



* The average o/p voltage is given by:

$$V_{dc} = \frac{2}{T}\int_0^{T/2} V_m \sin\omega t\, dt$$

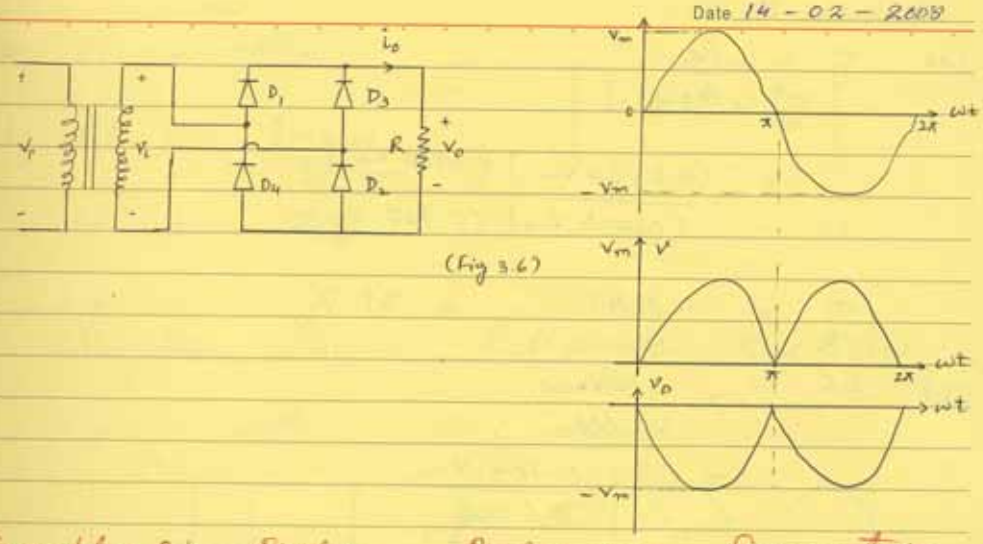


(Fig 3.5)

$$V_{dc} = \frac{2V_m}{\pi} = 0.6366\, V_m \qquad (3.21)$$

* Instead of using Center tapped trfr, we can use 4 diode bridge rectifier circuit as shown:

Date 14 - 02 - 2008



(Fig 3.6)

Example: 3.4 Finding Performance Parameters of a full-wave rectifier with center-tapped transformer.

↳ If rectifier in fig 3.5(a) has purely resistive load of R, determine (a) efficiency (b) FF (c) RF (d) TUF (e) PIV of D_1 and (f) CF of I/p current.

Solution:

$$V_{dc} = \frac{2V_m}{\pi} = 0.6366\,V_m$$

$$I_{dc} = \frac{V_{dc}}{R} = \frac{0.6366\,V_m}{R}$$

$$V_{rms} = \left[\frac{2}{T}\int_0^{T/2} (V_m \sin \omega t)^2\, dt\right]^{1/2} = \frac{V_m}{\sqrt{2}} = 0.707\,V_m$$

$$I_{rms} = \frac{V_{rms}}{R} = \frac{0.707\,V_m}{R}$$

Date

(a) $\eta = \dfrac{P_{dc}}{P_{ac}}$

$$= \frac{(0.6366\,V_m)\left(0.6366\,\frac{V_m}{R}\right)}{(0.707\,V_m)\left(0.707\,\frac{V_m}{R}\right)}$$

$\eta = 0.81 = 81\%$

(b) $FF = \dfrac{V_{rms}}{V_{dc}}$

$$= \frac{0.707\,V_m}{0.6366}$$

$= 1.1105$ or 111 %

(c) $RF = \dfrac{V_{ac}}{V_{dc}}$

$$= \sqrt{(1.1105)^2 - 1}$$

$RF = 0.483$ 48.3%

(d) TUF

$$V_s = \frac{V_m}{\sqrt{2}} = 0.707\,V_m$$

$$TUF = \frac{P_{dc}}{2V_s I_s}$$

$$I_s = \frac{0.5\,V_m}{R}$$

TUF = 0.57

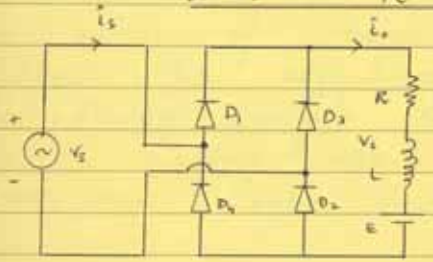
Date 14-02-2008

(e) $PIV = -2V_m$

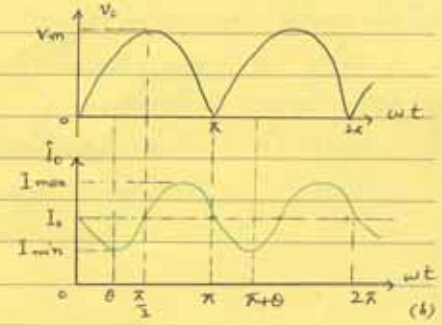
(f) $CF = \frac{I_{s(Peak)}}{I_s}$ $\left\{ I_{s(Peak)} = \frac{V_m}{R} \right\}$

$CF = 2$ Ans

Single Phase Full-wave Rectifier with R-L Load.

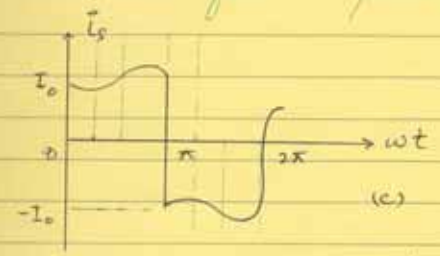


(a)



(b)

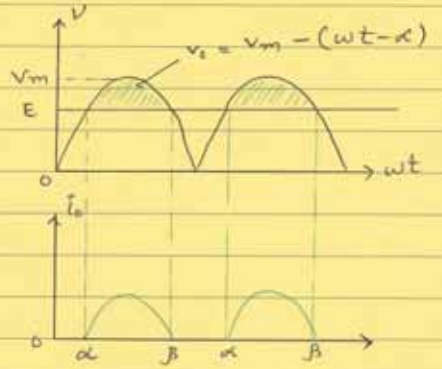
* Construction of Inverter this phenomenon is very useful to introduce an inductor.
* Because for pure Sine-wave o/p L makes it



(c)

Supply line Current

* 'L' is used where minute tuning is needed.



(d) Discontinuous Current.

Date 14-02-2008

* Two way controlling 'L' or 'L' o/p current can be changed continuous or discontinuous depends upon value of these elements.
* And gap b/w β to α will be filled by inductance variation.

Q: Consider a full wave rectifier that has been designed to supply $I_{dc} = 1A$ at 12 VDC compare the two possible designs for the implementation of set rectifier & compute the values of various performance parameters. Discuss the effect of increasing or dec't the Firing angle 'δ' if diodes w/e were are using are controllable devices.

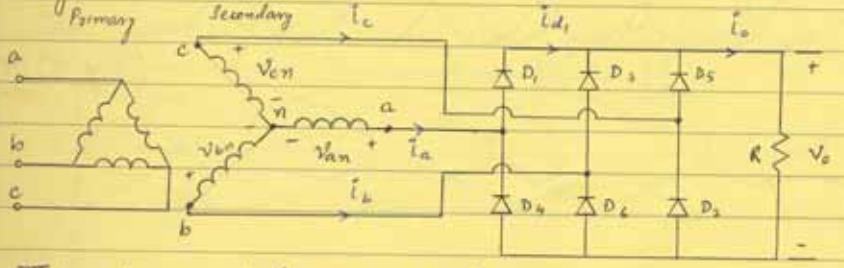
(Next week : before Wednesday class)

Date 20.02.2008

Introduction to Uncontrolled 3 Phase Rectification

* The 3 phase system provides good efficiency means optimal level of performance.

(Fig 3.13)



* This is a full wave rectifier.
* It can be operated with or without a tx/fr and gives six pulses ripples at output.
* Diodes are numbered in order of operational sequence.
* Each diode conducts for 120°.
* Diodes which are connected into supply lines with highest amplitude of line to line voltage will conduct.
* Six ripples per cycle.
* If V_m is peak value of phase voltage which is $V_L/\sqrt{3}$ is given by

$$V_{an} = V_m \sin(\omega t), \quad V_{bn} = V_m \sin(\omega t - 120^\circ)$$

$$V_{cn} = V_m \sin(\omega t - 240^\circ)$$

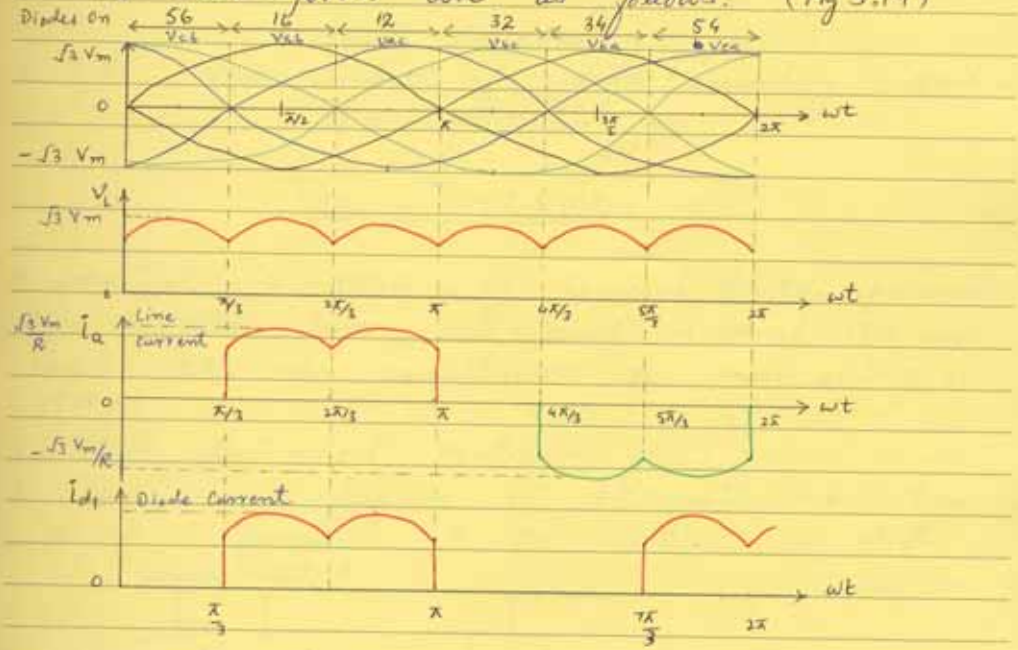
Date 20-02-2008

* The line voltages lead the phase voltages by 30° hence expression for line voltages.

$$V_{ab} = \sqrt{3}\, V_m \sin(\omega t + 30^\circ), \quad V_{bc} = \sqrt{3}\, V_m \sin(\omega t - 90^\circ)$$

$$V_{ca} = \sqrt{3}\, V_m \sin(\omega t - 210^\circ)$$

* The wave-forms are as follows: (Fig 3.14)



Conductions: B => D_3^+, D_6^- ; a => D_1^+, D_4^-

c => D_5^+, D_2^-

V_{bc} = D_3, D_2 ; V_{cb} = D_5, D_6

V_{ac} = D_1, D_2 ; V_{ca} = D_5, D_4

V_{ab} = D_1, D_6 ; V_{ba} = D_3, D_4

Date 21-02-2008

* The average output voltage is

$$V_{dc} = 1.654\ V_m$$

* The rms o/p voltage is given by:

$$V_{rms} = 1.6554\ V_m$$

* For a purely resistive load peak diode current is

$$I_m = \frac{\sqrt{3}\ V_m}{R}$$

* The rms diode current is:

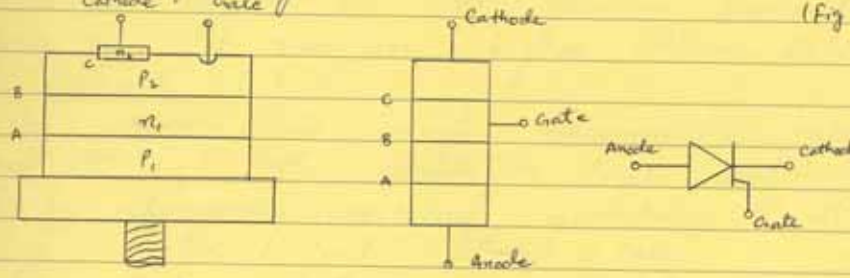
$$I_{rms} = 0.5518\ I_m \quad \Rightarrow 0.9557\ \frac{V_m}{R}$$

* The rms value of trfr secondary current is

$$I_s = 0.7804\ I_m$$

THE THYRISTOR

* Invented in 1957 by General Electric present day thyristor have rating of order of 1500 Amps and 10KV w/c corresponds to power rating of 15MW!
* Silicon Controlled Rectifier (SCR)
* Consist of layers of alternate P & N type semi-c forming 3 - PN Junctions as shown:



(Fig 2.1)

Date 21-02-2008

* When anode is +ve w.r.t cathode, junction A & C are forward biased whereas junction B is reversed biased and hence thyr can't conduct.
* Under the mode a forward leakage current is flowing through device.
* When anode voltage is further inc↑ to a value higher than V_{BO}, forward leakage current will reach saturation and reverse biased junction will breakdown.
* forward leakage current: Device is off
* Avalanch phenoma i.e. reversable in nature.
* This is called Avalanche Break down.
* After breakdown a high fwd current flows thru device w/c can only be limitted by external load.
* Under this condition voltage drop across device is 1 to 2V.
* Thyr shall behave as a conducting diode.
* If anode voltage is now dec↓ it shall have ~~not~~ no effect on this flowing current as long as it remain higher than latching current (I_L).
* If now fwd current becomes < holding current (I_h), the depletion layer would again start appearing arownd junction 'B' & thyr will enter fwd block state.
* If rated current is 40A, holding current is about 10mA.

Date 21-02-2008

* When anode is +ve w.r.t cathode, a small gate voltage can also Turn ON thyr as a small gate current starts to flow through layer's P_1 and P_2.

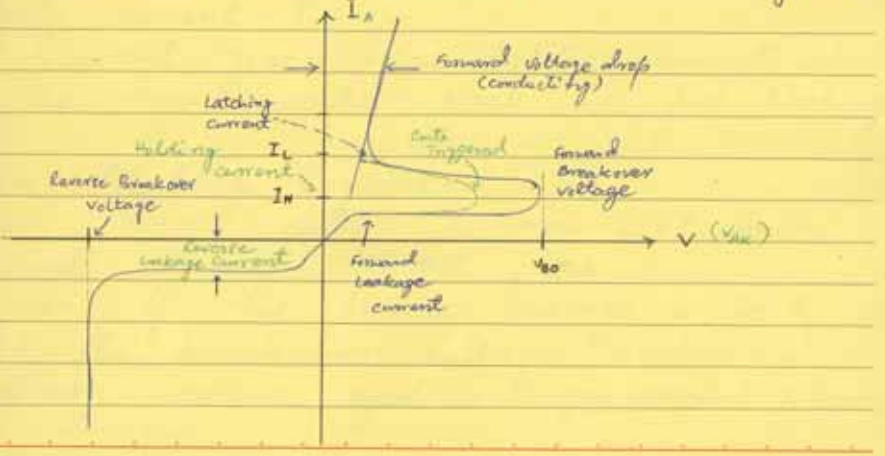
* There is no way to stop thyr if it is turned on by gate, it remains ON untill gate volt is zero. it has no effect on it.

* This method of switching is called gate control and perhaps most important method w.r.t thyr operation.

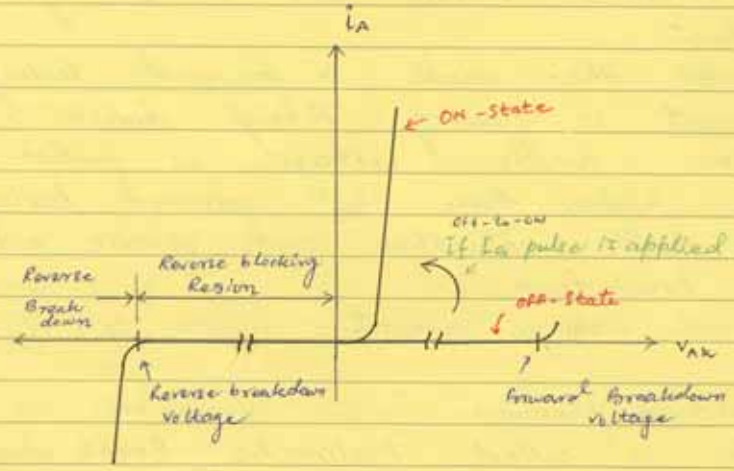
* If cathode is made +ve w.r.t anode, junction A and C shall be reversed biased and junction B forward biased. A small leakage current flows thru device & device is called the Reverse (break) Blocking state.

THE VI Characteristics

(Transfer characteristics) (fig 2.2)



Date H.W



* I_H = holding current to make device ready means devices is still conducting.

* I_L = The limit of current where SCR can drive load.

Date 21-02-2008

Regions of Operation

- Forward Blocking
- Forward Conducting
- Reverse Blocking.

Forward Blocking Region:

* The anode is +ve but anode voltage is less than the breakover voltage. A small forward leakage current flows but overall thyr remain Turn-Off.

Forward Conducting Region:

* Anode voltage is greater than breakover voltage
* Thyr conducts & a large forward current flows.
* The conduction can be achieved much prior to breakdown (over) voltage if the small gate current I_G is supplied. This would be called "Gate Controlled Turn ON" of the device
* The forward current must be more than latching current I_L.
* If current goes below holding current value I_h. The thyr switches back to fwd blocking state.

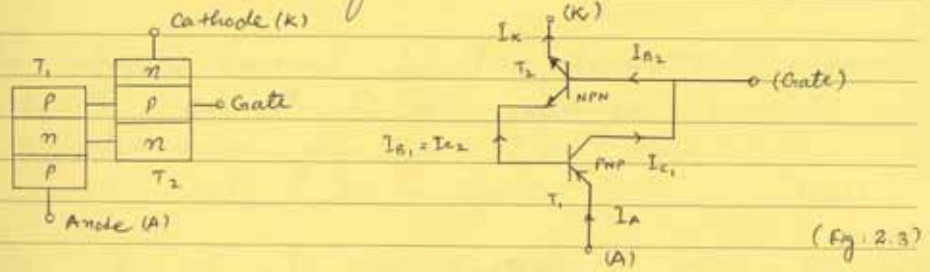
Reverse Blocking Region:

* Under this cathode is +ve w.r.t anode.
* A small reverse current flows.
* However if this reverse voltage is inc↑ beyond the breakdown voltage (avalanche) breakdown occurs and a large current flows thru device.

Date 21-02-2008

THE TWO TRANSISTOR MODEL OF SCR

* If we split middle two layers into two seperate parts each, as shown below we obtain Two transistor model of a SCR.



(Fig. 2.3)

* One transistor here is npn other is pnp trans.
* With no gate signal npn transistor would remain cut off with almost zero collector current
* I_c of npn trans. is actually base current for pnp trns. hence under no gate signal thyr is in forward block mode.
* A +ve bias at gate would turn npn trans ON.
* This in turn would establish I_c of npn trns w/c is I_b for pnp transistor.
* Hence pnp trans. would also turn ON. Now the I_c of Pnp trns. is actually I_b for npn.
* Thus an inc↑ of current in one trans. causes inc↑ of current in other and this cumulative action turns ON thyristor.
* Since I_c of pnp trans (w/c is also base current of npn) is much larger than gate

Date 21-02-2008.

current, hence once turned ON, gate loses control at device and thyr remains conducting even if gate bias is removed!.

* Hence gate bias can only turn ON SCR but it can't turn it OFF.

* The collector current I_c of a transistor is sum of emitter current I_E & leakage current of collector-base junction I_{CBO}. Thus

$$I_C = I_E + I_{CBO} \quad (2.1)$$

* The ratio of $\frac{I_C}{I_E}$ is denoted by α is known as "Current gain".
* for trans. T_1 emitter current is anode current I_A. Therefore, I_{C_1} of T_1 is

$$I_{C_1} = \alpha_1 I_A + I_{CBO1} \quad (2.2)$$

* where α_1 is current gain of T_1 and I_{CBO1} is leakage current of collector-base junction of T_1. Similarly the collector current I_{C_2} of T_2 is

$$I_{C_2} = \alpha_2 I_K + I_{CBO2} \quad (2.3)$$

* where α_2 is current gain, I_K is emitter current & I_{CBO2} is leakage current of C-B junction of T_2. The emitter current of T_2 is I_K.

From Eq (2.1) & (2.3)

$$I_A = I_{C_1} + I_{C_2} = \alpha_1 I_A + I_{CBO1} + \alpha_2 I_K + I_{CBO2} \quad (2.4)$$

Moreover

$$I_A + I_G = I_K \quad (2.5)$$

Date 21-02-08

Combing Eq (2.4) & (2.5)

$$I_A = \frac{I_{CBO1} + I_{CBO2} + \alpha_2 I_G}{1 - (\alpha_1 + \alpha_2)} \quad (2.6)$$

(Fig 2.4)

(Variation of α with I_E)

* Regenerative or +ve feedback.

* The junction capacitance affect thyr characteristics under transient conditions. Let thyr be in fwd blocking state. Fig 2.5 shows junction capacitance. The current i_B is

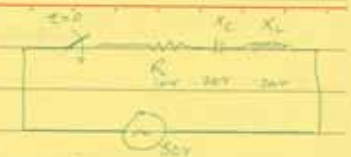
$$i_B = \frac{d}{dt}(q_B) = \frac{d}{dt}(C_B V_B)$$

$$i_B = V_B \frac{dC_B}{dt} + C_B \frac{dV_B}{dt} \quad (2.7)$$

(Fig 2.5)

Date 27-02-2008

* Transient Analysis.
* Steady State analysis



$$t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

* Stray capacitance effects on transient time or have a major role, will be dominent in transient time.
* C_B is more > than C_A & C_C
* Say I_B is leakage current of jn 'B'

Stray capacitance depends on several parameters like Anode voltage, cathode voltage ambient Temprature.

$$i_B = V_B \frac{dQ_B}{dt} + C_B \frac{dV_B}{dt}$$

(can be neglected)

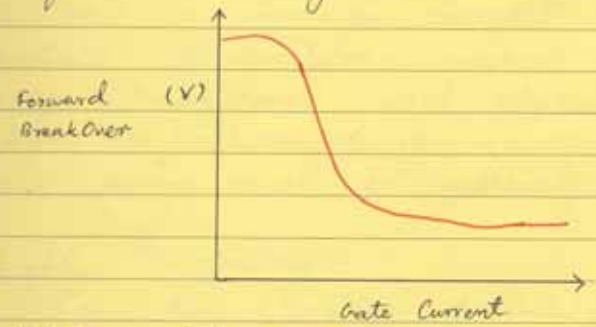
* where Q_B is change in junction B and C_B, V_B are junction capacitance & voltage as shown in Fig 25. If $\frac{dV}{dt}$ is high, current i_B would be high $\frac{dt}{dt}$. This would result in an inc↑ in leakage current I_{CBO1} and I_{CBO2} and cause thyr to turn ON. Moreover, high value of i_B may even damage the thyr.

Date 27-02-08

THYRISTOR TURN ON METHODS

- Also called "Triggering"
* Methods are:
  (1) Voltage Triggering (2) dV/dt --
  (3) Gate " (4) High Temprature -"-.
  (5) Light.

* ○ Voltage Triggering is seldom used as high voltage may destroy Thyr.
* ○ In gate ↔ forward breakover voltage shifts with gate current as shown:



* DV/dt Triggering:
* The reverse biased jn (J B) behaves as a capacitor under forward blocking mode.
* If a rapidly changing voltage is applied across Anode and Cathode of thyr, a charging current 'I_B' flows thru device from A to K. This charging I directly depends upon rate of change of voltage or Transient voltage as shown by following equation.

$$I_B = C_B \frac{dV}{dt}$$

Date 27-02-2008

* Greater voltage transient, greater current I_B greater forward current. This higher forward current may cause turning on of thyr.
* This method is not suitable for SCR triggering either as high I_B would result in high fwd current that may damage SCR.

o High Temprature triggering:

* As temprature of a p-n junction inc↑ width of depletion layer decr. This is due to reason that number of electron hole pairs is inc↑ & leakage current inc↑. At a certain temprature reverse biased junction may breakdown and thyr starts conducting. High temprature triggering may cause thermal run away and it generally avoided.

o Light Triggering:

* In this method particles (neutrons or photons) are made to strike reverse biased junction. This cause an inc↑ in number of electron-hole pairs and triggering of thyr. This method of triggering is used in light activated silicon controlled rectifier (LASCR) and light activated silicon switch. (LASCS).

Date 27-02-2008

Gate Control

An easy method to switch ON SCR into conduction state is to apply proper +ve signal to gate. This signal should be applied when thyristor is forward biased and should be removed after device has been switched ON. The turn on time is about 1 – 4 μsec. This gate signal can be dc, ac and pulse.

(28-02-2007)

Gate signal can be: AC Signal, Pulse, DC voltage

(a) DC Gate Signal: The application of a dc gate snl causes flow of gate current & triggers SCR. The disadvantage of this method is that snl has to be continuously applied resulting in power loss. Moreover, gate control ckt is not isolated from the main power circuit.

(b) AC Gate Signal: In this method a phase-shifted ac voltage derived from main supplies the gate signal. The instant of firing can be controlled by phase angle control of gate signal.

Natural de-activation of gate

(c) Pulse: In this method SCR is triggered by application +ve pulse of correct magnitude. A power electronics circuit has a number of thyrs connected in series & ||.

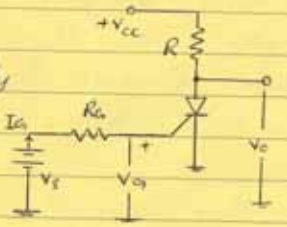
- A pulse has a regulated wave-form of a fixed duration. It can be +ve or -ve. They have to be switched on at proper

Date 28-02-2008

instants in a certain sequence. This can be done by a train of high frequency pulses applied to proper instant through a logic circuit. A pulse transformer is used for isolation. In this method gate losses are very low b/c drive is discontinuous.

Trigger Current and Trigger Voltage

The actual source voltage needed for triggering depends on gate circuit. In fig 18 gate circuit current I_G flows through a resistance R_G. It is seen that



$$V_S = V_G + I_G R_G \quad \text{--- (29)}$$

Thyristor Specification and Ratings

VOLTAGE RATINGS

(a) Peak working off state fwd voltage (V_{DWM}):
Known as peak working fwd blocking volt, this is ~~right~~ max^{m} value of (fwd) volt. w/c thyr can withstand when it is in off state. All repetitive and non-repetitive transient voltage are ~~exact~~ excluded from this definition.

(b) Peak repetitive off-state fwd volt (V_{DRM}):
It is max^{m} value of fwd voltage w/c thyr can withstand when it is off-state & volt is applied repeatedly. This voltage is specified at a max^{m} allowable jns temprature. A thyr has to withstand such a voltage when it is turned off.

Date 28-02-2008

(c) Peak impulse fwd blocking voltage (V_{DSM}):
It is max value of any non-repetitive surge voltage w/c thyr can withstand when is turn-off state.

(d) Peak working reverse voltage (V_{RWM}): It is max value of rev. volt w/c thyristor can withstand. (Repetitive and non-rep transient volt are excluded from this definition.

(e)
It is max value of reverse volt. w/c may be applied repeatedly to thyr.

(f)
It is max. transient rev volt w/c thyr can withstand. If a diode having same rating as thyr is connected in series with it, the peak voltage across thyr is reduced.

(g) On state Voltage (V_T):
It is V.drop across thyr (ie b/w A & K) at specified value of fwd current & jns Temprature. It is about 1 - 1.5 V.

(h)
It is max^{m} gate voltage required to cause gate triggering current.

(i)
It is max^{m} rate of rise of a A. voltage w/c will not trigger thyr, if gate sml is

Date 28-02-2008

applied. It is evident that $\frac{dv}{dt}$ is more than rated value, thyr may be turned ON. As discussed previously a high $\frac{dv}{dt}$ can turn ON a thyr. even if absence of gate signal, due to flow of charging current.

(j) Voltage safety factor:

The actual rev. volt across thyr should be less than V_{RSM} under all conditions of operation. To ensure the device doesn't get damaged, a safety factor of about 2 is used. This safety factor is defined as

$$\text{Voltage safety factor} = \frac{V_{RSM}}{\sqrt{2}\,(\text{RMS i/p voltage})} \quad \text{--- (2.10)}$$

(eg Jacket factory: Medium size)
(max-size, min-size)

Tolerances: (i) Long-term (ii) Short-term.

CURRENT RATING

(a) Average on state (fwd) Current (I_{TAV}):

Sine vdrop across a conducting thyr is low, current I_{TAV} determines power loss in Thyr. For same average current but different conducting periods, peak I and different and therefore, the jnx temprature are different. Therefore, permissible voltage average current should be decr with incr in period of conduction. The current I_{TAV} depends on temprature of case & data sheets of manufacturer

Date 28-02-2008

indicated this fact.

(b) RMS ON state current (I_{RMS}):

Even if actual average value of fwd I is less than specified value, the heating may exclusive. This is ½c of reason that heating depends on effective (RMS) current and not average I. Therefore, an rms value of fwd current is also specified for max jnx temprature.

(c) Impulse (surge) current rating (I_{TSM}):

In addition to rated steady state current a thyr is also subjected to Surge I under abnormal conditions. This current is max. surge I (non-repetitive) c/c thyr can withstand.

* Maximum AC handling capability (I_{RMS})
* " DC " capability ($I_{max\ avg}$)

(d) I^2t Rating:

It is max. non-repetitive value of square of instantaneous current integrated over time. Thus it indicates energy that device can absorb without getting damaged. It is usually specified for overloads lasting less than one half cycle. This rating is necessary co-ordinate working of thyr with operation of a fast acting fuse used to protect thyr agains overloads.

Response time - I^2t
(Fuse rating)

Date 28-02-2008

(e) dv/dt rating :

This rating indicates maximum allowable rate of inc↑ of anode I. When thyr is triggered, conduction initially starts near cathode and then spreads to whole jn. If dv/dt is very high, conductivity may not be able to spread as fast and local hot spots may occur. This may raise temprature beyond permissible limit. The safe value of $\frac{dv}{dt}$ lies in range of 50 to 800 A/μ sec. A special type of thyr known as Amplifying Gate Thyristor can withstand very high $\frac{dv}{dt}$. Moreover, a thyr using a hard drive gate circuit can withstand high $\frac{dv}{dt}$.

(e) Holding Current (I_h):

It is max. A 'I' at w/c thyr can continue conducting. If anode become less than I_h, thyr is turned OFF. This current is in mA range.

(f) Latching Current (I_L):

when gate current is applied to a thyr (in fwd blocking mode), 'A' current starts inc↑, Latching current is mini↓ anode 'I' to keep thyr in conducting state after gate pulse is removed. This 'I' is about two to 3 times holding current.

(g) Max & Min Gate current:

The minimum gate current indicates that value of gate current w/c is sufficient to turn ON thyr. The mini↓ gate current depends on

Date 28-02-08

rate of rise of 'A' current. The max gate 'I' indicates safe value of gate current. Gate 'I' should not exceed the max value.

POWER RATINGS

(a) Forward Conduction loss:

The average fwd conduction loss equals product of average 'A' current and V.drop across thyr. For same value of average 'A' current, this loss inc↑ with ↓dec in period of conduction. This loss is a major portion of losses in a thyr.

(b) Turn ON loss:

During turn ON process, V.drop across a thyr is pretty high, Therefore appreciable power loss occurs during Turn ON period.

(c) Turn off loss:

During rapid off, reverse current may be as high as fwd conduction 'I'. To limit this loss an extra inductance is added in circuit. However, this inductance may cause high rev. volt transient. In high frequency ckts thyr are turned ON and OFF many times in each cycle of mains frequency. In such cases Turn ON & OFF losses may be appreciable.

(d) Forward blocking (leakage) loss:

This loss occurs when a fwd volt is applied but thyr is not conducting. A fwd

Date 05-03-2008

leakage current flows during this period. It is product of fwd blocking volt & fwd leakage current. This loss is small.

(e) Reverse blocking (leakage) loss:
This loss occurs when Rev voltage is applied. It is equal to product of rev. voltage and rev leakage current. This loss is also small.

(f) Gate Power loss: This loss equals product of gate voltage & I_G. Most thyr ckts use pulse signals for triggering. For such system gate power loss is negligible.

TEMPRATURE Ratings

(a) Junction temprature (T_j): The jns temprature determines ability of thyr to operate sucessfully. If jns tmpratdre goes beyond specified value, thyr may start conducting even if gate signal is not applied. The fwd breakover volt turn off time and thermal stability depends on jns temprature.

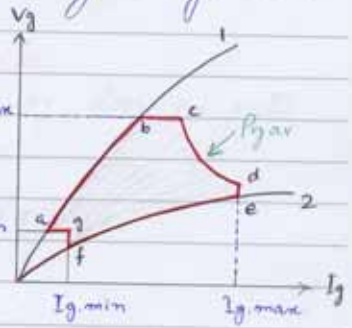
(b) Thermal resistance: The heat dissipation from cooling surface depends on the thermal resistance it is expressed in unit of temprature difference (°C) per watt of power dissipated.

Date 05-03-2008

Selection of Parameters of Triggering Circuit

Gate Characterstics

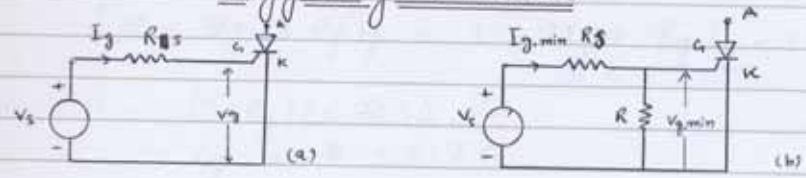
* It is a graph b/w gate voltage (V_g) and gate current (I_g)
* Two curves for two extreme conditions are shown below.
* $P_g = V_g I_g$
* It is also shown in following diagram:



* The operating are here is abcdefga.

Consider that:
Case: 1 max. Ig and min Vg
Case: 2 max Vg and min Ig

Triggering Circuits



* Fig 2.20(a) show the simplest triggering circuit

$$V_s = V_G + I_G R_s.$$

* Fig 2.20(b) shows triggering circuit after resistance 'R' has been added b/w gate & cathode. This resistance is connected to provide a path for leakage current Taking min value of V_g & I_g as $V_{g\,min}$ & $I_{g\,min}$

Date 05-03-2008

, We get

$$V_s = \left(\frac{V_{g.min}}{R} + I_{g.min} \right) R_s + V_{g.min}$$

Example 2.4: The $V_g - I_g$ characteristics of an SCR is given by $V_g = 1 + 9 I_g$. The gate pulses are rectangular with voltage amplitude of 12 V and duration 60 μsec. The duty cycle is 0.3

(a) Find series resistance R_g in gate ckt to limit peak power loss to 6W.

(b) Find average gate power loss.

Solutions (a) Since a peak power loss in gate circuit is $V_g I_g$, we have

$$6 = V_g I_g = (1 + I_g 9) I_g$$

or $$9 I_g^2 + I_g - 6 = 0$$

$$I_g = 0.763 \text{ A}$$

KVL equation of gate circuit is

$$12 = V_g + R_g I_g = 1 + 9 I_g + R_g I_g = 1 + (9 + R_g) I_g$$

$$11 = (9 + R_g)(0.763)$$

$$R_g = 5.417 \ \Omega$$

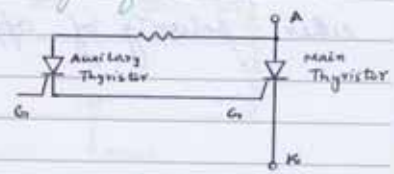
(b) Average power loss = $6 \times 0.3 \Rightarrow 1.8$ Watt

Date 06-03-08

Methods of to improve di/dt and dv/dt Ratings of Thyristor

* Base of construction of SCR & biasing of it

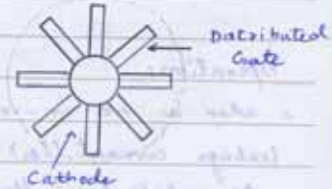
Auxilary Thyristor to improve the $\frac{di}{dt}$ Rating:



* The higher gate current greater current handling capability
* As resistance of SCR is inversly proportional to Anode to Cathode current.

Intermixing of Gate & Cathode regions

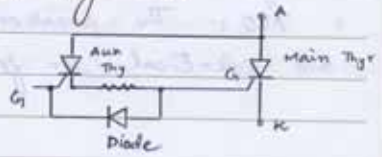
* As size of cathode region is large, larger the current capability
* If gate region is deposited within the cathode region
* So instead of making single gate in cathode many distributed gates are added in cathode so di increase can be handled well.



Distributed gate config.

Gate Assisted Turn-off Thyristor

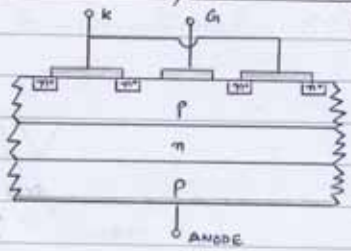
Turn off time: 10μs, $V_{BO} = 2000$V.
On state Current = around 1500 A



* Increase in voltage (A-K) causes leakage current from (G) and no path to flow (dissipate) the leakage current

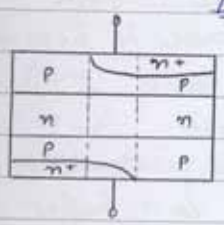
Date 06-03-2008

Cathode Shorts to increase dv/dt Rating

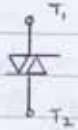


* It is the current that is formed due high voltages at A-k damages the scr not the high voltages.
* By this technique current have several different ways (external paths) to flow heavily.

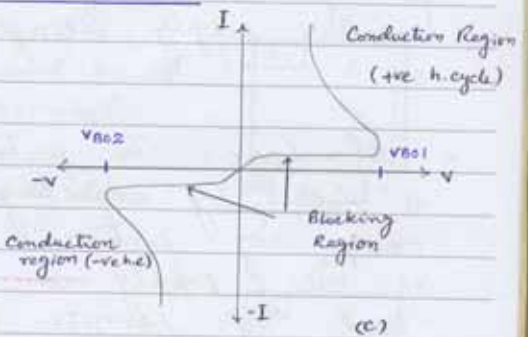
DIODE FOR AC (DIAC)



(a)



(b)

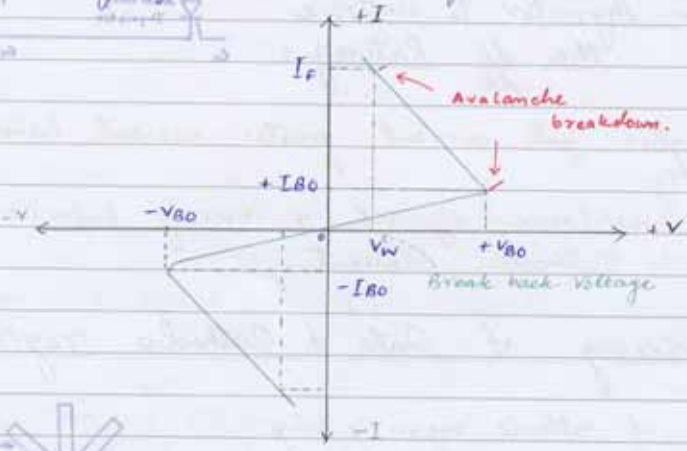


(c)

* V_{BO} for common Diac is about 30V.
* It only conducts when only V_{BO} is reached.
* Typical application is for triggering Triacs. A triac requires a +ve or -ve pulse to trigger it ON. the diac provides same.
* Matched Diac / Triac combinations are manufactured by a number of manufacturers

Date 4/10

DIAC: A two terminal, three layer bidirectional device w/c can be be switched from its OFF state to ON for either polarity of applied voltage.



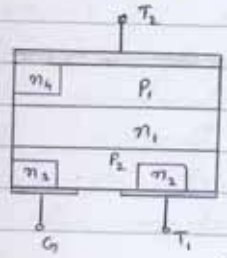
Operation:

- when a +ve or -ve voltage is applied across diac, only a small leakage current (I_{BO}) will flow through device.
- As applied voltage is inc't leakage current will continue to flow until voltage reaches breakover (V_{BO}).
- At this point avalanche breakdown of reverse-biased jns occurs and device exhibits -ve resistance i.e current through device inc't with dec't values of applied voltage. The voltage across device then drops to break back (V_W) voltage.
- Note: The breakover voltage and holding current values are identical for forward and reverse regions of operation.

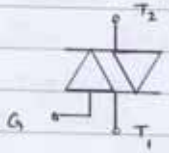
Date 06-03-2008

TRIACS (TRIODE FOR AC)

THE Bi-Directional SCR



(a)



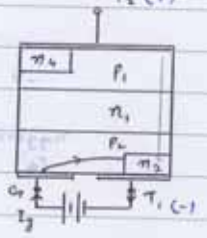
(b)

* It conduct in both direction. $T_1 \rightarrow T_2$ / $T_2 \rightarrow T_1$
* There is overlapping of Terminals.

First Quadrent Operations:

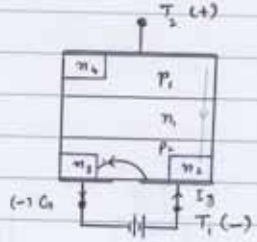
MODE-1

* P_1-n_1 and P_2-n_2 forward biased
* n_1-P_2 breaks down, normal current starts to flow.
* Gate is no biased slightly less than T_2.



MODE-2

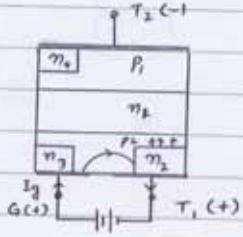
* Initially : P_1-n_2, P_2-n_3
* After current flow P_1-n_1-P_2-n_2



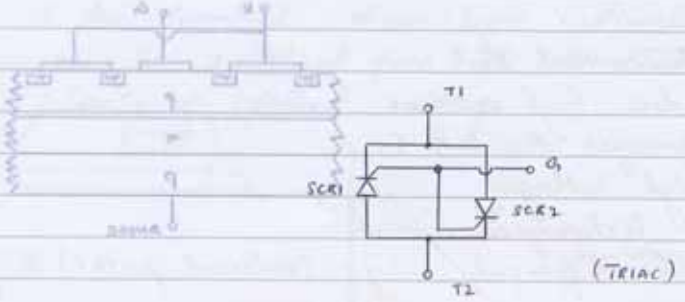
Third Quadrent Operations:

MODE-3

* P_2-n_1-P_1-n_4, n_1-P_1 breaks down current starts to flow thru above path.
* Third quadrant operation high gate

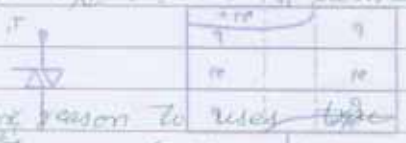


Date H.W



(TRIAC)

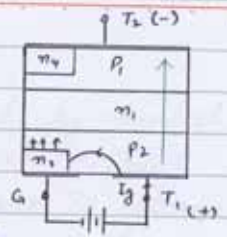
* The supply voltage at w/c triac is turned ON depends upon gate current Ig. The greater gate current smaller supply voltage at w/c triac is turned ON.



* Advantage: The feature or reason to used triac is that by adjusting gate current to a proper value any portions of +ve and -ve half-cycle of a.c supply can be made to flow through load. This permits to adjust transfer of a.c power from source to load.

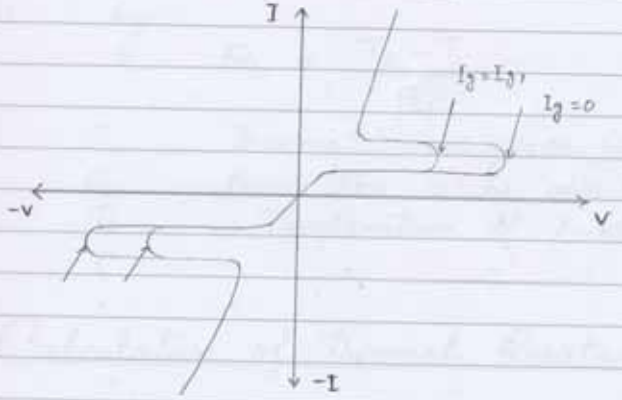
Date 06-03-2008

MODE - 4

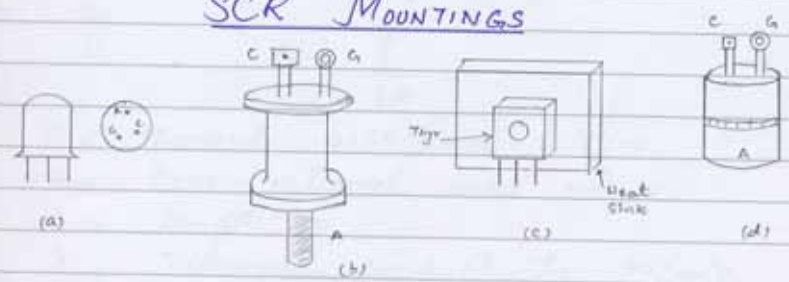


* $P_2 - n_1 - P_1 - n_4$, $n_1 - P_1$ breaks down current starts to flow thru above path.
* 3rd quadrent operation lower gate current is required to turn-ON triac. Its more sensitive in this mode.

V-I characteristics



SCR MOUNTINGS



Date 06-03-2008

Thermal Ohm's Law

The heat dissipation is governed by thermal ohm's law. As per analogy with electric circuit theory, temprature difference is analogue to voltage difference, heat is analogue to charge and thermal resistance is analogue to electrical resistance.

As per thermal ohm's law, heat dissipation is given by

$$\Theta_{21} = \frac{T_2 - T_1}{P_{21}}$$

where
Θ_{21} = Thermal resistance b/w point 2 & 1.
P_{21} = Power loss to be dissipated from "
T_2 = Temperature of point 2 °C.
T_1 = " " " 1 °C.

Calculation of Thermal Resistance:

* The thermal resistance of material is given by

$$\Theta = \frac{l}{\lambda A}$$

where
Θ = thermal resistance in °C/W
A = Cross-sectional area, m^2
l = length, m
λ = Thermal conductivity, W/m°C.

* A material used commonly for heat sinks is 90% aluminium having conductivity of 220 W/m°C.

Date 06-03-2009.

HEAT SINKS

* Greater no of fins, greater the volume, greater heat dissipation.
* Today Aluminium alloys are formed.
* Heat sink should be light in weight.
* Should not melt with high temprature increase.

Example 2.17: Find thermal resistance of square cross section aluminium rod having length 0.2 m width 0.01m and depth 0.01 m. Thermal conductivity is 220 w/m°C. If temrature at far end is 30°C find temprature of surface where heat is injected and cube has power dissipation of 3 watt?

Solution: Thermal resistance

$$\theta = \frac{0.2}{220 \times 0.01 \times 0.01}$$

$$\theta = 9.091\ ^\circ C/W$$

$$T_2 = (P)\theta + T_1$$

$$= (3)(9.091) + 30^\circ$$

$$T_2 = 57.27^\circ C$$ ✓

Example 2.18: An electronic device is mounted on an aluminium plate having length 2 mm and area of cross section 120 cm^2 it is desired that temprature drop along 2 mm length should be 4°C. Take thermal conductivity of Al as 220 w/m°C. Find max losses w/c can be handled by module.

Date

Practice Assignment:

Q/ Assume that for same heat sink module:
(A) The volume inc↑ 3 times.
(B) " " dec↓ 3 times.

* Evaluate (comment) on the changes in electrical loss (P) and thermal resist. 'θ' for the two cases. x——x

Q Example 2.19: A thyr has a power dissipation of 30 W. Assume max junction temprature 125°C and max ambient temprature of 50°C. The thermal resistance of thyr is 1°C/W. The device uses a 65 μm thick mica insulator having thermal K of 0.3 °C/W. Find thermal resistance of heat sink and select a proper heat sink.

Solution:

$$\text{Total thermal } R = \frac{\text{Temprature diff}}{\text{Power dissipated}} = \frac{125-50}{30}$$

$$" \quad " = 2.5\ ^\circ C/W$$

Thermal resistance of heat sink = 2.5 − 1 − 0.3

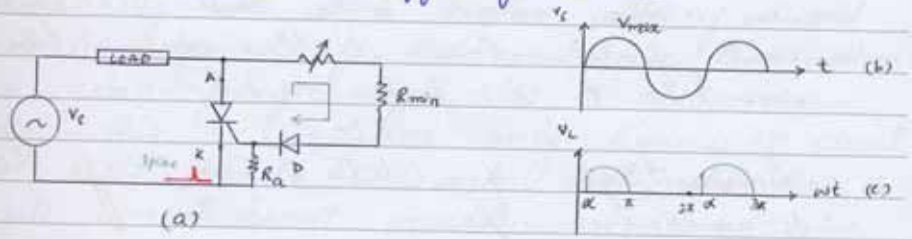
" " " = 1.2 °C/W

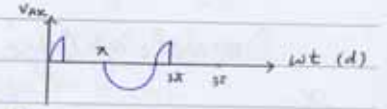
Heat sink no. 10 in fig 9.32 has a thermal resistance of 1.2 °C/W and is suitable for this purpose. ✓

Date 12-03-2008

Triggering Circuits

"Resistance Triggering Circuit"





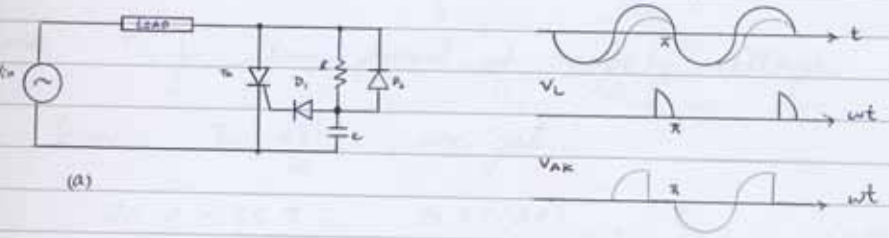
1. When voltage V_s starts its +ve half cycle, thyristor become fwd biased. However it start conducting only when its gate current I_g min exceed. During this +ve h.cycle Diode, G-K jns of SCR also become fwd biased.
2. As V_s inc↑, G current inc↑, I_g becomes more than $I_{g(min)}$ SCR start conducting. when SCR conducts, V drop across it is very small. Therefore almost total voltage V_s appears across load.
3. SCR continues to conduct full current since it is more than holding current. Since holding current is very small (a few mA only). SCR conducts almost ($wt = \pi$)
4. At $wt = \pi$, a reverse voltage appears SCR and it turns OFF.
5. The diode in G-ckt does not allow G-K reverse bias to exceed peak rev. voltage during +ve h.cycle. PIV rating of diode should

Date 12-03-08

become more than V_{max}. (Atleast twice).

* The firing angle 'α' can be controlled by varying R. if R is more, I_g will attain value $I_{g(min)}$ at a higher value of α and conduction period of SCR would be lower. when R is zero, firing angle α is also min. Under this condition only R_{min} is in circuit. The R_{min} should be such that, when R=0, the gate current doesnot exceed max allowed value.

RC Triggering Circuit 'Half Wave'



* Variable R & C adjust time constant or Turn On Time of SCR!

* During -ve h.cycle of V_s, Cap charges to V_{max} with lower plate +ve through diode D_2. The volt across Cap is equal to V_{max} at $wt = 90°$ The cap voltage remains at this value (or may decr slightly) as source voltage changes from V_{max} at $wt = -90°$ to zero at $wt = 0$, V_s starts its +ve h.cycle, cap starts charging rev direction

Date 12-03-2008.

through resistance R. The rate of charging of cap in +ve h.cyc. is controlled by R. when volt across cap has become +ve and equal to $V_{g(min)} + V_{D1}$ (where V_{D1} is V.drop across D_1). SCR is triggered, after caps voltage remain at this same value during remaing +ve h.cycle. In next cycle process is reapeted. D_1 prevents rev breakdown of gate.

An empirical relation for product RC is

$$RC \geq 0.65\,T$$

where $T = \frac{1}{f}$ time period of supply voltage.

Since $T = \frac{2\pi}{\omega}$, we get

$$RC \geq 0.65\,T = \frac{0.65(2\pi)}{\omega} = \frac{4}{\omega} \quad \text{—(2.18)}$$

SCR will trigger when cap voltage V_c is $V_c = V_{g(min)} + V_{D1}$. The instantaneous value of V_s at instant of triggering is

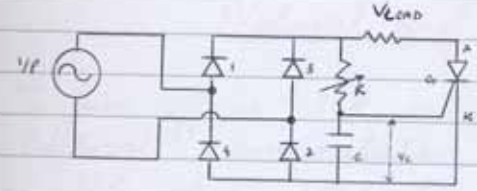
$$V_s \geq \left(I_{g(min)} * R\right) + V_{g\,min} + V_{D1}$$

$$R \leq \frac{V_s - V_{g(min)} - V_{D1}}{I_{g(min)}} \quad \text{—(2.19)}$$

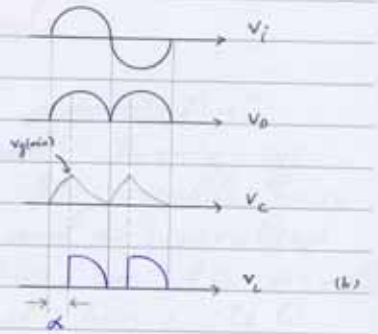
The values of R & C can be found from eq 2.18 and 2.19.

Date 12,03,08

RC Turn ON 'Full wave Type'



(a)



(b)

During +ve h.c diode 1 and 2 conducts During -ve h.c diode 3 and 4 conducts Thus we get bridge o/p V_L as shown in fig 2.38 (b) This voltage chdrges cap 'C' through variable R. The voltage across cap V_c as in figure. when value of V_c reaches a value equal to min gate trig voltage, thyr is trigd in each half cy. The firing angle α can be controlled by using 'R'. The load voltage V_L is also shown. Since there is no diode across resistance in this case eq (2.19) calculating value of R changes to.

$$R \leq \frac{V_s - V_{g(min)}}{I_{g(min)}} \quad \text{—(2.19)}$$

Date 13-03-2008

Commutation of SCRs

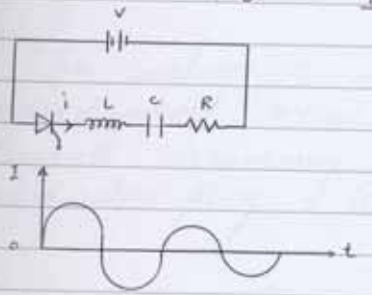
"Natural and Forced"

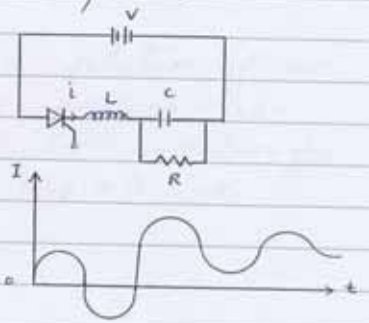
* To turn off a SCR is called "commutation".
* Natural commutation means turning off of SCR when current thru it reaches zero level or polarity across A and K reverses. This naturally happens when an AC signal is applied (passed) thru it hence its called natural commutation.
* Forced commutation means turning off SCR thru external circuitary.
* Components inductances & capacitances are used to attain forced commutation and hence are called 'Commutating Components'.
* Forced comtn can be classified into class A, B, C, D and E depending upon arrangement of commutating elements used to achieve comtn and method of to achieve zero current and reverse voltage across SCR to turn it off.
* Classification is based on config of components and circuit or config of 'C' and 'L' in circuit defines class of circuit.

Date 13-03-2008

Commutation of SCRs 'Class - A'

or Reasonent Response





* Identification of class A is that max load current flows thru comt components as series circuit of comt components is made.
* Oscillator is found to cross zero.

Case 1: when load is in series with L & C.

$$i = \frac{V - V_0}{\omega_d L} e^{-\zeta \omega_n t} \sin(\omega_d t) \qquad (2.25)$$

The current reaches zero at

$$\omega_d t_0 = \pi \quad \text{or} \quad t_0 = \frac{\pi}{\omega_d} = \frac{\pi}{\left(\frac{1}{LC} - \frac{R^2}{4L^2}\right)^{0.5}} \qquad (2.26)$$

where

$\omega_n = \frac{1}{\sqrt{LC}}$:= natural frequency.

and

$\zeta = \frac{R}{2\sqrt{L/C}}$:= damping ration

and $\omega_d = \omega_n \sqrt{1 - \zeta^2}$

Date 13-03-2008

* When current is zero at time t_0, comtn of thyr can take place.

The analysis is well known solution of an underdamped circuit. ω_d is known as damped frequency of osc. The condition for underdamping is that $\omega_d > 0$ or

$$\frac{1}{LC} - \frac{R^2}{4L^2} > 0$$

or

$$R < \sqrt{\frac{4L}{C}} \qquad (2.27)$$

Case 2: when load is in Parallel with C.

$$i = \frac{V}{\omega_d L} e^{-\xi\omega_n t} \sin(\omega_d t) + \frac{V}{\omega_d RLC} e^{-\xi\omega_n t} \ldots$$

$$\ldots \left[\frac{-\xi\omega_n \sin(\omega_d t) - \omega_d \cos(A)}{\omega_n^2}\right]$$

where $(A = \omega_d t)$ (2.29)

where $\xi = \frac{1}{2R\sqrt{C/L}}$:= damping ratio

$$\omega_n = \frac{1}{\sqrt{LC}}$$

and

$$\omega_d = \omega_n \sqrt{1-\xi^2}$$

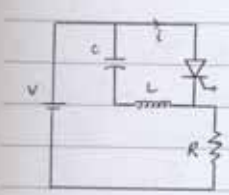
fig shows waveform of current. At a certain time current reaches zero value & comt. thyr can be done.

Date 13-03-2008

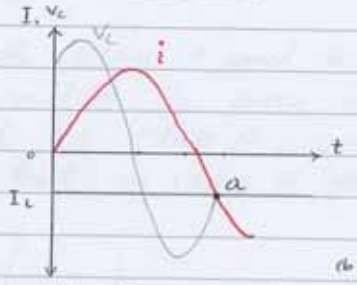
Commutation of SCRs 'Class - B'

or

Self Commutation



(a)



(b)

* In this class no max load current flows thru comt. components. (Diff b/w class A & B)

* Initially capacitor gets charged to battery 'V' with upper plate +ve. As soon as thyr is turned on, it starts conducting and supplying current to load 'R'. Now cap starts discharging through L and thyr (The path of this 'I' is thru Thyr, L and back to C.). After getting completely discharged, it starts getting charged with opposite polarity (i.e lower plate +ve) D/c of this rev voltg a -ve current starts flowing. This -ve current opposes load current. At point 'a' in fig (b) load current and -ve comt 'I' are equal and thyr is turned Off. Once thyr is turned off cap starts getting charged again (thru L & R) with upper plate +ve, thus SCR remains off for some time, then remains on for some time & this cycle is

Date 13-03-2008

is repeated. The time for ON & OFF on value of L & C.

* It is seen that both class A and B comtn methods are similar to some extent. The main diff is that in class A, comtg elements carry load but in class B this is not so,

$$i = \frac{V}{\frac{1}{\sqrt{LC}} L} \sin\left(\frac{1}{\sqrt{LC}}\right)$$

$$i = V\sqrt{\frac{C}{L}} \sin\left(\frac{1}{\sqrt{LC}}\right) \qquad (2.32)$$

The peak value of comtn corent is

$$I_{c(peak)} = V\sqrt{\frac{C}{L}} \qquad (2.33)$$

The cap voltage is

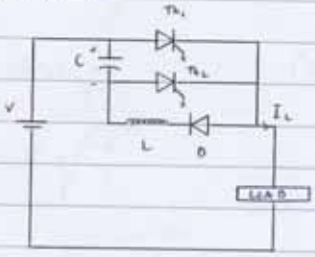
$$V_c = V\left(1 - \cos\frac{1}{\sqrt{LC}}\right) \qquad (2.34)$$

* After a time $t = t_0 = \pi\sqrt{LC}$ charging current becomes zero and thyr is switched Off, the waveforms of I and V_c are shown in fig (b).

* Due to inductor voltage of ckt can be greater the supply voltage thats way L is added in ckt.

Date 13-03-2008

Auxilary Commutation 'Class C'



* Assume cap is initially charged to V_c with upper plate +ve and lower -ve.
* MODE 1: When main thyr is trigd. I_L thru load flows, mean while cap also begins to discharge thru D, Th_1 and L.
* At end of this mode Cap is charged to opsite polarity. The diode D prevents its discharging in opt. polarity.
* MODE 2: For turning off main thyr, aux thyr is triggered.
* This allows opst. charged cap to get discharged thru main thyr Th_1.
* While doing so, current flows thru cathode to A of main thyr.
* This turns Off main thyr.
* As main thyr ceases conduction, rev current also stops and hence aux thyr also stops.
* At end of this mode Cap is charged in original polarity i.e. upper plate +ve and lower -ve and cycle repeats.

Date 13-03-08

When Th_1 is turned ON, oscillatory current thru C, D and L is given by

$$i_c = V\sqrt{\frac{C}{L}}\sin\frac{t}{\sqrt{LC}} \qquad (2.36)$$

Peak cap o/p current $= V\sqrt{\frac{C}{L}}$

* This current must be < max current of Th_1. If this max current is denoted by I_{max} we have

$$V\sqrt{\frac{C}{L}} < I_{max}$$

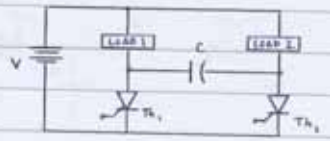
or

$$L > \frac{V^2C}{I_{max}^2} \qquad (2.37)$$

Complementary Commutation 'Class D'

MODE 1:

Thyr Th_1 is turned ON by a gate pulse. Load current flows from battery to Load 1 thru Th_1. Along with a cap charging current flows from battery thru load 2, cap and thyr Th_1. This current charges cap to battery voltage V with polarity as shown in fig.



Date 13-03-2008

MODE 2: A gate pulse is applied to thyr Th_2 turning it ON. The cap voltage now appears as rev bias across Th_1 and a charging current flows from battery thru load 1, cap and Load 2. This charging current charges to cap to V_s with rev voltage (rev polarity)

When thyr Th_1 is turned ON in next cycle, volt across cap rev biases thyr Th_2 and turn it off. The action of events is repeated in subsequent cycle.

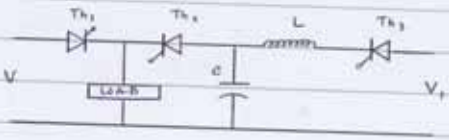
$$t_{off} = R_1 C \ln 2$$

Precaution: V_c should be $\geq V_s$ to turn off Th_1 otherwise no use of this technique

External Pulse Commutation 'Class E'

MODE 1:

Thyr Th_1 is turned ON It supplies load from voltage source 'V'.



At the same time Th_2 is also turned ON. A current pulse having a peak value $V_1\sqrt{C/L}$ flows from source V_1, thru Th_2 and L and charges cap to $2V_1$. The no. of LC sections can also be more than one. If 'n' is no. of LC sections duration

Date 13-03-2008

of current pulse will be $\pi\sqrt{LC}$. when cap is charged, charging current decr↓ to zero and the thyr Th_3 is turned off.

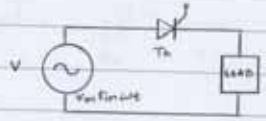
MODE 2: Thyr Th_2 is trigd. The cap voltage appears (aeross) as rev bias at Th_1 and turns it off. The capacitor discharges thru load.

The above two mode are regd in each cycle.

Line Commutation 'Class F'

CAUTION!

The turn off time of thyr must be less than negative half cycle.



Date 19.03.2008

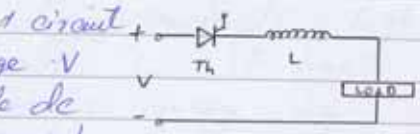
Protection of Thyristors

* Reasons:

① A SCR has to be protected from:
- Over Current
- " Voltage
- High dv/dt
- " di/dt.

(a) di/dt Protection:

o Fig 2.51 shows a simple chopper circuit in w/c a fixed dc voltage V is converted into a variable dc voltage by controlling the ON & Off periods of thyr. The di/dt in circuit can be controlled by including an 'L' in ckt. The max di/dt in circuit is



(fig 2.51)

$$\frac{di}{dt} = \frac{V}{L} \qquad (2.43)$$

Precaution:

Inappropriate value can incr losses power losses.

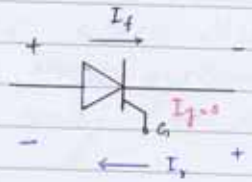
Date 19.03.2008

(b) Overvoltage Protection:

* Why over voltage occur in circuit?

Causes of Over-voltage:

* Thyr Commutation.
* Current chopping
* Lightening
* Trfr in-rush current



1. Thyristor Commutation:

when a thyr turn off. a reverse current flows to sweep away the stored charge. This reverse current inc to its max value & then decays at a high rate. This high di/dt induces a high over voltage L di/dt to cirt 'L'. It has been found that this over-V may be much higher then rated value and may demage thys.

2. Current Chopping:

when a small current is interrupted by a ckt breaker. current may be brought to zero abruptly and ahead of normal current zero. This known as Current Chopping and is often observed when no load current of a trfr is switched off. Current chp often leads to dangerous over voltages.

(Diagram)

Date 19.03.2008

3. Lightning:

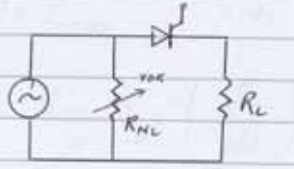
HVDC systems are fed by high voltage transmission lines. Atmospheric lightning causes high magnitude over-V w/c travel on lines as travelling waves. When these waves reach converter station HVDC system, thyristor in converter station may be subjected to these over-voltages.

4. Transformer in Rush Current:

when a trfr is switched ON initial magnetising current may be higher than steady state value of mag current. If a thyr circuit is connected on secondary side of trfr, thir may be subjected to over-voltage b/c trfr sec. voltage b/c of in-rush magnetising current may be upto about twice rated sec voltage.

(6) Over voltage Protection:

$$i = k v^{\alpha} \qquad (2.44)$$

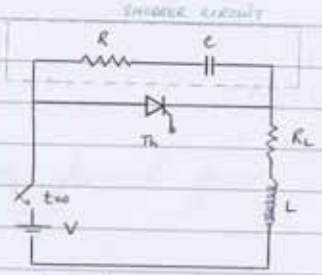


* Voltage Dependent Resistor

Date 20, 03, 2008

(c) **Snubber Circuit :**

dv/dt Protection



o When circuit of fig 2.52 is switched on at $t=0$ cap behaves as a short ckt (b/c voltage across cap can't change instantaneously). Moreover, thyr is in fwd blocking state and has therefore a very high resistance. Therefore, only resistances R and R_L & L in ckt.

Hence KVL equation is

$$V = (R+R_L)i + L\frac{di}{dt}$$

(↳ Condition : valid for very short time)

The voltage across thyr at $t = 0$ is Ri :

i.e $$V = Ri$$

or

$$\frac{dv}{dt} = R\frac{di}{dt}$$

$$\left(\frac{dv}{dt}\right)_{max} = R\left(\frac{di}{dt}\right)_{max} = \frac{V}{L}$$

or

$$R = \frac{L}{V}\left(\frac{dv}{dt}\right)_{max} \quad \text{....(2.50)}$$

The ckt consisting of R, R_L, L & C is

Date 20, 03, 2008

always designed to be critically damped. For a critically damped ckt parameters are required as :

$$R + R_L = 2\sqrt{\frac{L}{C}} \quad \text{(2.51)}$$

→ The values R & C can be found from Eqns (2.50 and 2.51)

* Snubber is a form of critically damped system as critically damped system has fastest response.

* In an AC ckt parameters R and C can be found from eqs (2.50 and 2.51) by substituting max value of voltage in place of 'V'.

A useful formula to find C is

$$C = 10\frac{VA}{V_s^2}\left(\frac{60}{f}\right) \quad \text{(2.52)}$$

where

VA := Full load rating of ckt
V_s := Applied voltage
f := Frequency (H_z)

* Resistance of Snubber

$$R = 2\zeta\sqrt{\frac{L}{C}} \quad \text{....(2.53)}$$

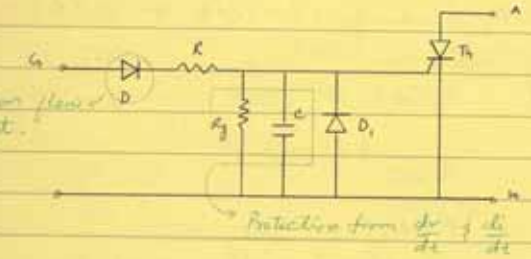
Date 20.03.2008

* L := Effective inductance

when max value of $\frac{dv}{dt}$ is specified, C is given by

$$C = \frac{1}{2L}\left[\frac{0.564\,V_m}{dv/dt}\right] \qquad (2.54)$$

(d) Gate Protection :



Example 2.26. In an AC ckt using thyr having di/dt 25 V/μs, source L = 0.2 mH. The rms value of V_s = 230V. If damping factor is 0.65 find value of R & C of snubber circuit.

Sol.

$$V_m = 230 \times \sqrt{2} = 325.27\,V$$

$$L = 0.2 \times 10^{-3}\,H$$

$$\frac{dv}{dt} = 25\,V/\mu s = 25 \times 10^6\,V/s$$

$$\zeta = 0.65$$

Using eq (2.54)

$$C = \frac{1}{2 \times 0.2 \times 10^{-3}} \times \left[\frac{0.564 \times 325.27}{25 \times 10^6}\right] = 134.6 \times 10^{-6}\,F$$

Date 20.03.2008

Example 2.29: V_s = 300V R_L = 10Ω, L=0 f = 2000 Hz $\frac{dv}{dt}$ = 100 V/μs i = 100A (a) R=?, C=? (b) power loss. (c) power rating of snubber.

Sol:

(a) By KVL eq during charging of cap C (fig 2.52) is

$$V = (R+R_L)i + \frac{1}{C}\int i\,dt + V_c(0)$$

As = that $V_c(0)$ is zero,

So,

$$i = \frac{Ve^{-t/(R+R_L)C}}{R+R_L}$$

The fwd voltage across thyr is

$$V_{Th} = V - R_L i = 300 - \frac{10\,Ve^{-t/(R+R_L)C}}{R+R_L}$$

At $t=0$

$$V_{Th} = V - \frac{R_L}{R+R_L}V$$

At $t = \tau = (R+R_L)C$

$$V_{Th} = V - \frac{0.369R_L}{(R+R_L)}V$$

$$\frac{dv}{dt} = \frac{V_{Th}(\tau) - V_{Th}(0)}{\tau} = \frac{0.632R_L V}{C(R+R_L)^2}$$

Date 20, 03, 08

$$R = \frac{300}{100} = 3\Omega$$

$$\frac{dv}{dt} = 100 \times 10^6 = \frac{0.632(10)(300)}{C(3+10)^2}$$

$$C = \frac{0.632(10)(300)}{13^2 \times 100 \times 10^6} = 0.112 \times 10^{-6} f$$

(or) $C = 0.112\ \mu f$

Example 2.30: $R = 4\Omega$, $L = 6\mu H$, $C = 6\mu F$, $V = 300V$ find max permissible values of $\frac{dv}{dt}$ & $\frac{di}{dt}$?

Sol $\left(\frac{di}{dt}\right)_{max} = \frac{V}{L} = \frac{300}{6 \times 10^{-6}} = 50 \times 10^6$ A/s

when ckt is switched ON rate of change of voltage across cap is

$$\frac{dv_c}{dt} = R\frac{di}{dt} + \frac{I_{sc}}{C}$$

I_{sc} = short circuit current $= \frac{300}{4} = 75A$

$$\frac{dv_c}{dt} = 4 \times 50 \times 10^6 + \frac{75}{6 \times 10^{-6}}$$

$$\frac{dv_c}{dt} = 212.5 \times 10^6 \text{ V/s}$$

Hence max permissible value of $\frac{dv}{dt}$ 212.5×10^6 V/sec.

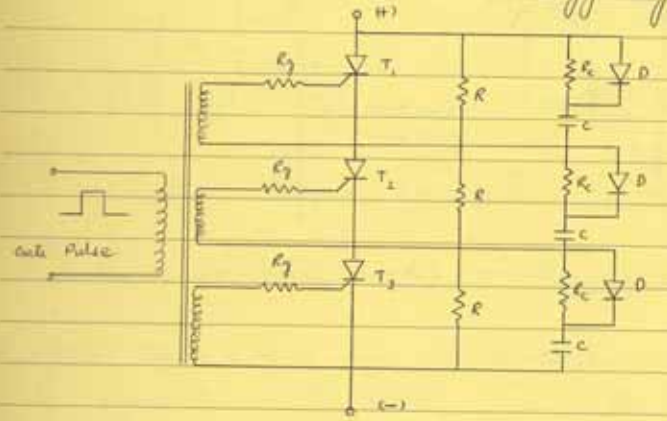
Date 20.03.2008

Thyristors in Series

Methods available:

* Simultaneous.
* Sequential.
* Optical.

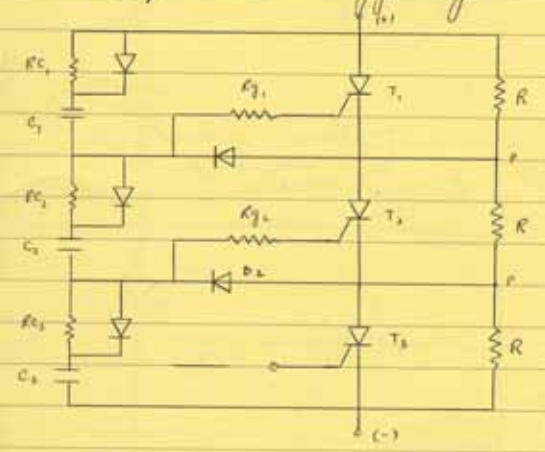
Simultaneous Triggering



* Pulse Trxfr : Allows pulse to transform.
  - Core is special
  - Small in size relatively.
* A specialized trxfr is needed for this method.
* Tappings required as no of thyr are in ckt

Date 26.03.2008

Sequential Triggering



Path 1: $C_3^+ - R_{C_3} - R_{g_2} - T_{2(G-K)} - T_{3(A-K)} - C_3$

Path 2: $C_2^+ - R_{C_2} - R_{g_1} - T_{1(G-K)} - T_{2(A-K)} - D_2' - C_2$.

* Above two Path of Discharge current P_1 and P_2 causes T_2 and T_1 to Triggger.
* In this method Capacitor is more sensitive.

$$C \geq \frac{10}{R_g + \frac{E_{GT(max)}}{I_{GT(max)}}} \mu F \qquad (4.10)$$

where,

$E_{GT(max)}$:= Max gate trig Voltage
$I_{GT(max)}$:= " " Current
R_g := gate - source resistance

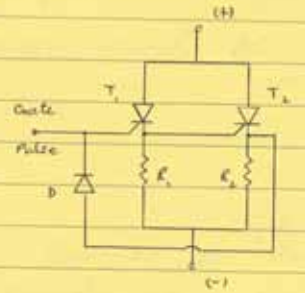
Date 26.03.08

Optical Triggering

Diagram

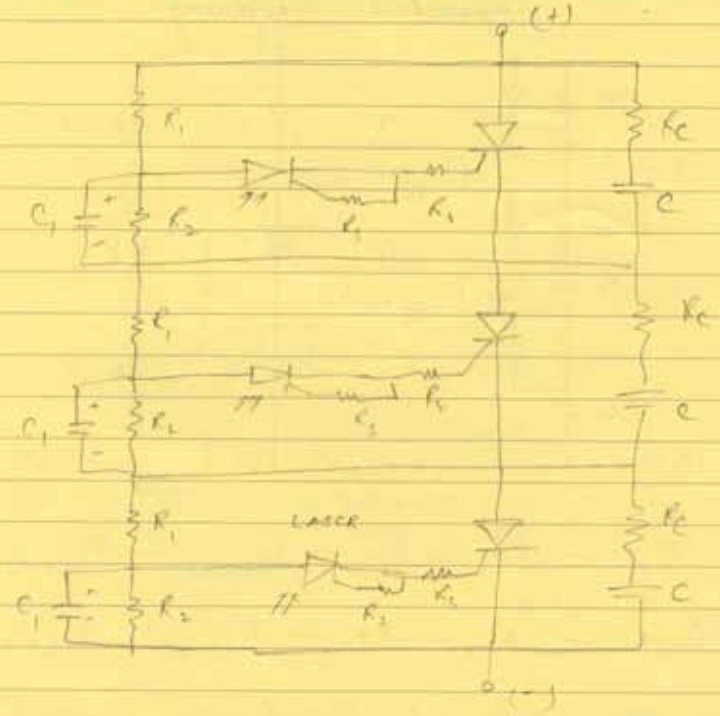
* LASER : Problem - Electro static charge these should be separated electrostatically.

Thyristors in Parallel



* In case T_1 is off (say) the connection from $T_2(K)$ to $T_1(G)$ from Diode (D) insures that T_1 is switched ON.
* Diode ensures that if T_1 tends to turn off (may be due to its anode current becoming lesser that I_H) it will be ON again by V across R_2.

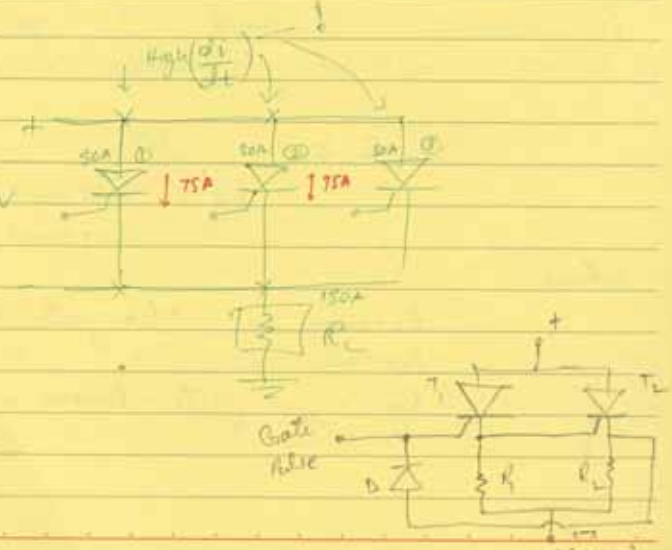
Date



Two problems:

(1) $\frac{di}{dt}$

(2) Load division.



(Diagram)

Date 27.03.2008

AC VOLTAGE CONTROLLERS

(AC Regulators)

* O/P voltage < I/P voltage. (For this Topic)

* It converts an AC voltage in variable AC voltage of same frequency.

* Applications:
  - → Industrial heating.
  - → Illumination level controller. (Dimmer)
  - → On load tx/r tap changing
  - → Speed control of induction motor.

* Older alternative methods for AC voltage level control:
  1. Auto tx/r.
  2. Tap changing tx/r.
  3. Saturable reactance.

* Advantages of Thyr or triac based AC controllers
  - ↳ High η
  - ↳ Fast control
  - ↳ Compact size

* The only dis-advantage however is that they introduce Objectionable harmonics in circuit!

Date 27.03.2008

* Classification of AC controllers:
  (1) Single ϕ (Half or Full wave)
  (2) 3 ϕ (. .)

* Single ϕ are actually Unidirectional and full wave are bi-directional.

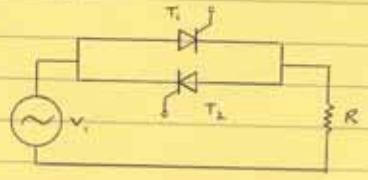
* Natural commutation is seen in AC controllers, no need of forced commutation.

* Types of AC controllers:

  (1) Integral cycle control (ON/OFF)
  (2) Phase control.

Principle of Integral Cycle Control

* This method is also called 'ON/off control'.
* AC supply connected to load from some cycles and it is disconnected from load for another no. of cycles.
* On and off times consist of an integral no. of cycles.
* Zero crossing Gate turn on is adopted.



(a)

Date 27.03.2008

Let I/p voltage be

$V_i = V_m \sin \omega t$

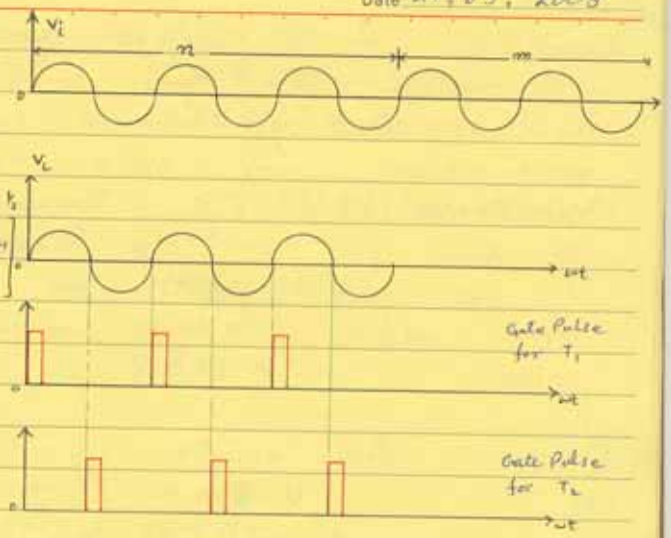
The rms value of o/p voltage is

$$V_L = \left[\left(\frac{n}{n+m}\right)\frac{1}{2\pi}\int_0^{2\pi} V_m^2 \sin^2 \omega t \, d\omega t\right]^{0.5}$$

or

$$V_L = \frac{V_m}{\sqrt{2}}\left(\frac{n}{n+m}\right)^{0.5}$$

$$V_L = V\sqrt{\alpha}$$



* V_L and V are rms values of o/p and I/p voltages

↳ The ratio $\left(\frac{n}{n+m}\right)$ is duty cycle 'α'.

* It is customary to keep sum $n+m = 100$.
* Method suitable for loads having high mechanical inertia and high thermal constant like industrial heating and speed control of motors.
* Period of control is '$(n+m)T$' where 'T' is time period of AC cycle.
* This period should be less than mechanical or thermal time constant.

Date 27.03.2008

Example 6.1: An ac voltage regulator uses integral cycle control. The thyrs conduct for 36 cycles and remain off for 64 cycles. The rms value of i/p = 150 V and load resistance is 8 Ω. Find:
(a) Rms V_L (b) o/p Power (c) i/p power (d) i/p power factor (e) average and rms value of thyr current. Neglect losses.

Sol:

As

(a) $$V_L = \frac{V_m}{\sqrt{2}} \left(\frac{n}{n+m}\right)^{0.5}$$

or

$$V_L = V_{s\,rms} \left(\frac{n}{n+m}\right)^{1/2}$$

$$= 150\,(0.6)$$

$$V_L = 90 \text{ V}$$

(b) Power o/p $= \frac{(90)^2}{8} = 1012.5$ W

(c) Neglecting losses o/p power = i/p power = 1012.5 W

(d) RMS Current (load) $= \frac{90}{8} = 11.25$ A

$$VA = 150 \times 11.25$$

$$= 1687.5 \text{ VA}$$

$$\text{Input pf} = \frac{1012.5}{1687.5} = 0.6 \text{ Lagging}$$

Date 27.03.08

(e) Peak thyr current $= \frac{\sqrt{2} \times 150}{8}$

$$= 26.5165 \text{ A}$$

Average thyr current $= \frac{\alpha}{2\pi} \int_{\pi}^{2\pi} (26.5165) \sin \omega t \, d(\omega t)$

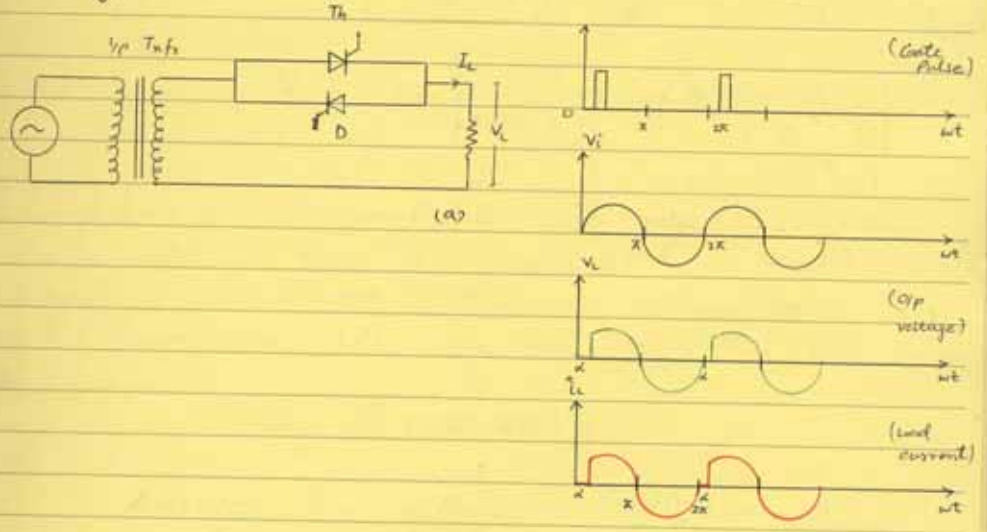
$$= \frac{0.36 \times 26.5165}{\pi}$$

$$= 3.038 \text{ A}$$

RMS SCR I $= \frac{26.5165}{2} \sqrt{0.36}$

$$= 7.954 \text{ A}$$

Single ϕ Half-wave Ac Controller



(b)

Date 27.03.2008

Input voltage is $V_i = V_m \sin \omega t$

The average o/p voltage is given by:

$$V_{av} = \frac{1}{2\pi}\left[\int_{\alpha}^{2\pi} V_m \sin \omega t \, d(\omega t)\right]$$

or

$$\boxed{V_{av} = \frac{V_m}{2\pi}(\cos\alpha - 1)}$$

The rms value of o/p voltage is

$$V_L = \left[\frac{1}{2\pi}\int_{\alpha}^{2\pi} V_m^2 \sin^2 \omega t \, d(\omega t)\right]^{0.5}$$

or

$$V_L = \left[\frac{V_m^2}{4\pi}\int_{\alpha}^{2\pi} \frac{1-\cos 2\omega t}{2} \, d(\omega t)\right]^{0.5}$$

$$* \quad V_L = V_m\left[\frac{1}{4\pi}\left(2\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{0.5}$$

Example 6.2: A single ϕ h.w regulator $V_{in} = 150V$, $R_L = 8\Omega$, $\alpha = 60°$ in each +ve h. cycle. Find (a) P_{av} (b) V_{rms} o/p (c) Power o/p (d) I/p Pf (e) I_{av} over 1 cycle.

Sol

$$V_m = \sqrt{2} \times 150 = 212.1 \text{ V}$$

(a)

$$\text{Average o/p voltage} = \frac{212.1(\cos 60° - 1)}{2\pi}$$

$$= -16.878 \text{ V}$$

Date

$$V_L = 212.1\left[\frac{1}{4\pi}\left(2\pi - \frac{60\pi}{180} + \frac{\sin 120°}{2}\right)\right]^{0.5}$$

$$= 142.45 \text{ V}$$

(c) Power o/p $= \frac{142.45^2}{8} = 2536.50$ W

(d) o/p Current = I/p current $= \frac{142.45}{8}$

$= 17.806$ A

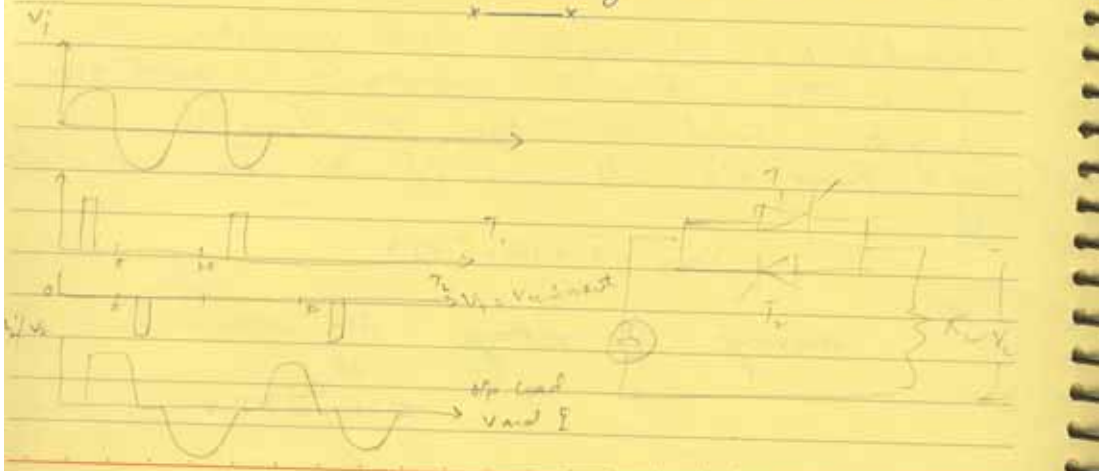
I/p VA $= 150 \times 17.806$

$= 2670.9$ VA

I/p Pf $= \frac{2536.50}{2670.9} = 0.949 \approx 0.95$ Lagging

(e) Average I/p current = Average o/p current

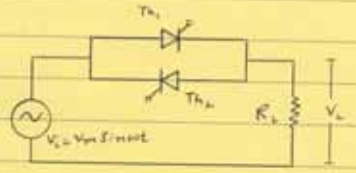
$$= -\frac{16.878}{8} = -2.10 \text{ A}$$



Date 27.03.2008

Single Phase Full-wave AC Regulator / Controller

Caution: Gate ckts for Two thyrs need to be isolated!



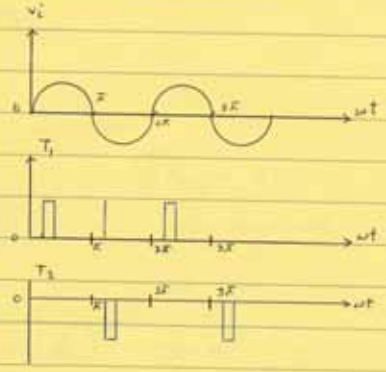
Vav is:

$$V_{av} = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin\omega t \, d(\omega t)$$

(or)

$$V_{av} = \frac{V_m}{\pi}\left|-\cos\omega t\right|_{\alpha}^{\pi}$$

$$V_{av} = \frac{V_m}{\pi}\left(1+\cos\alpha\right) \quad \ldots(6.4)$$



Rms o/p voltage:

$$V_L = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2\omega t \, d(\omega t)\right]^{0.5}$$

$$= \frac{V_m^2}{2\pi}\int_{\alpha}^{\pi}\left(1-\cos 2\omega t\right) d(\omega t)$$

(or)

$$V_L = V_m\left[\frac{1}{2\pi}\left(\pi-\alpha+\frac{\sin 2\alpha}{2}\right)\right]^{0.5} \quad \ldots(6.5)$$

Date 02.04.2008

Single Phase Full-wave AC Controller

Some more Configurations

* Gate circuits need not to be isolated. During +ve h cycle Th1 and D1 conducts, during -ve h cycle Th2 and D2 conducts. Power consumption of this ckt is higher than previous case.

(Page 82)

* After every alternate cycle TRIAC is to triggered again.

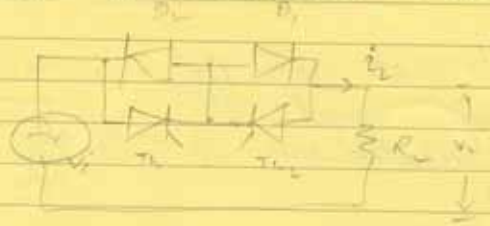
Single ϕ Full-wave AC Controllers

R-L Load

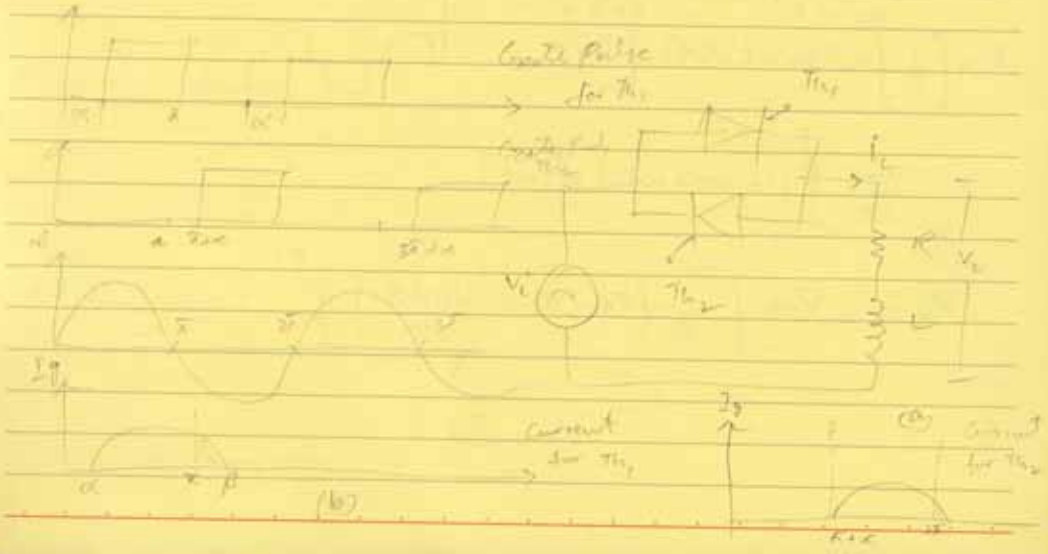
P-82

Date

* Say back to back SCRs are connected firing ckt is same for them in case both are triggered same time this is reduced in this ckt

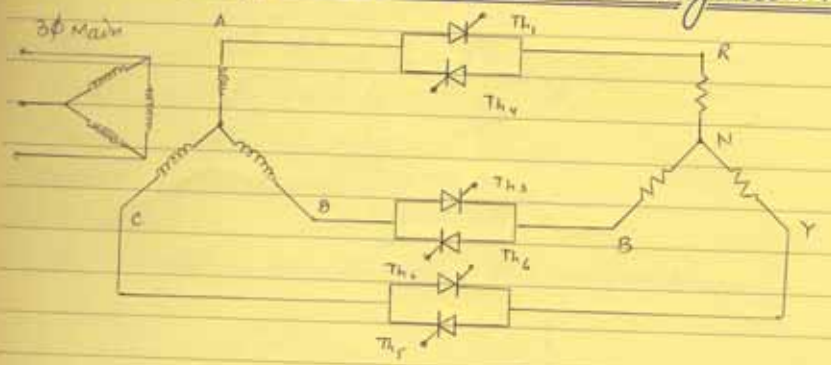


(Single ϕ regulator using TRIAC)



Date 03.04.2008

3 ϕ Full-wave AC Regulators



* $V_L = \underbrace{\sqrt{3}\, V_m \left[\frac{1}{\pi} \left(\frac{5\pi}{24} - \frac{\alpha}{4} + \frac{\sin 2\alpha}{16} + \frac{\sqrt{3}\cos 2\alpha}{16} \right) \right]}^{0.5}$

3-ϕ Full-wave AC Controllers

Other possible Connections

Tie Connection :

* Neutral is connected with control circuit
* load is on star and supply is delta

Date 03.04.2008

Delta connections:

* This connection used where no possibility to change type of system means no star is available.
* 'α' should be same ∀ phases.

CYCLOCONVERTERS

* Essentially a frequency converter.
* A single step process in wfc we don't convert AC – DC then again AC.
* Converters / regulators convert fixed AC into variable or fixed AC output voltage but frequency remains the same.
* A cyclo-converter gives variable AC voltage with diff frequency!
* One way of accomplishing is a two step operation, first conversion of AC - DC then converting DC into diff freq AC thro inversion!
* By using a cycloconverter this 2 step process can be avoided and made more simple!.
* A cyclo converter converts AC of one freq into other without involving DC conversion processes.

84

Date 03.04.2008

Delta connections:

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CYCLOCONVERTERS

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* By using a cycloconverter this 2 step process can be avoided and made more simple!.
* A cyclo converter converts AC of one freq into other without involving DC conversion processes.

Date 03.04.2008

* Hence its an AC-AC converter with diff freq without any intermediate DC link.

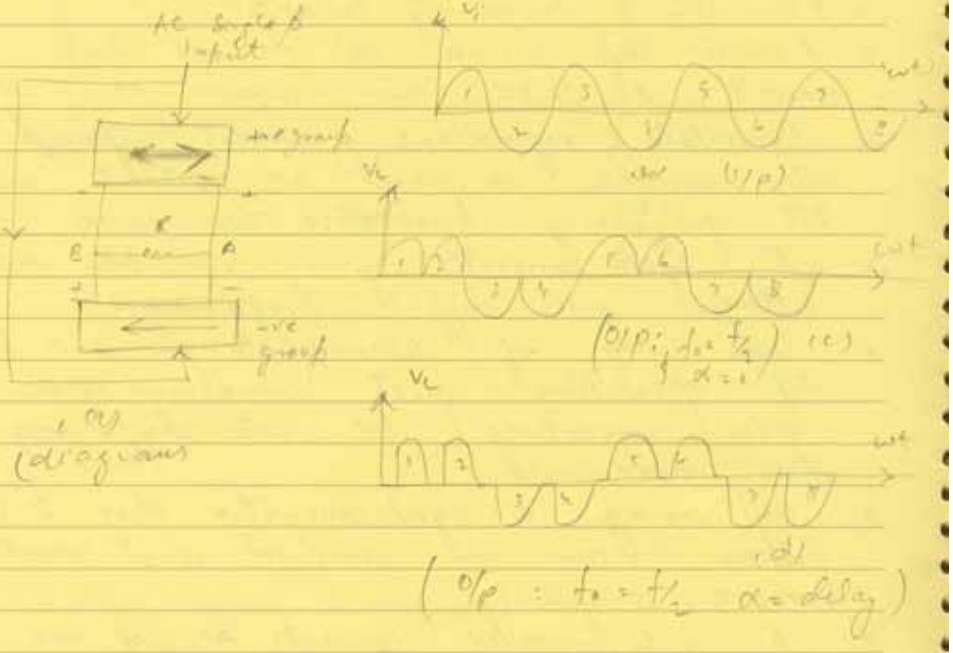
Types:

(1. Single ϕ to Single ϕ
(2. 3ϕ to single ϕ
(3. 3ϕ to 3ϕ

* These can be step up or down.
* Step up would mean o/p freq is higher than i/p.
* Step down vice versa.
* " " uses natural or line commutation whereas step up uses forced commutation.
* They were initially developed for electrical traction. (eg Conveyor belt, electric locomotive)
(Physical movement of heavy load using electrical energy.

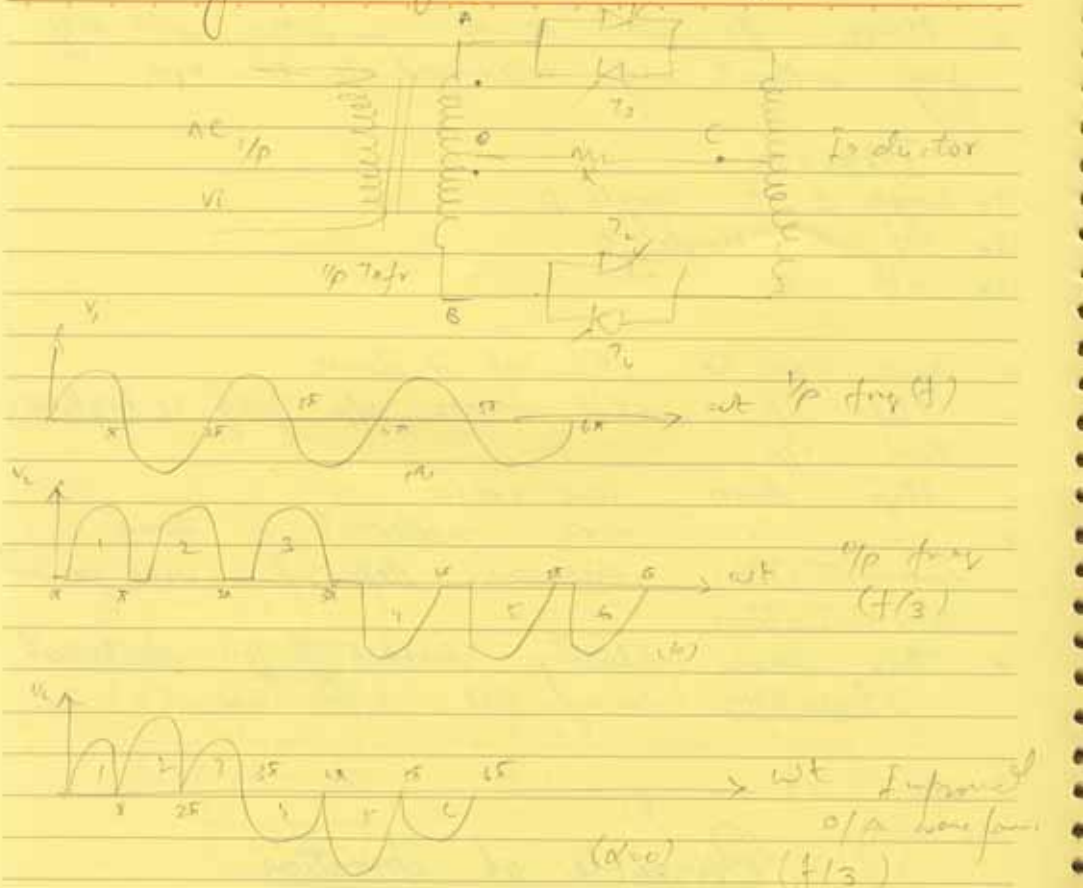
Principle of operation

Date



Single ϕ cycloconverter Cetre Tapped

Date



No of half cycle i/p	Thyr T_{h_1}	Path of I	Direction of I thru load
1	T_{h_1}	A - T_{h_1} - C - O - A	C to O
2	T_{h_2}	B - T_{h_2} - C - O - B	C to O
3	T_{h_1}	A - T_{h_1} - C - O - A	C to O
4	T_{h_3}	O - C - T_{h_3} - O	O to C
5	T_{h_4}	O - C - T_{h_4} - O	O to C
6	T_{h_3}	O - C - T_{h_3} - O	O to C

Date 05.04.2008

INVERTERS

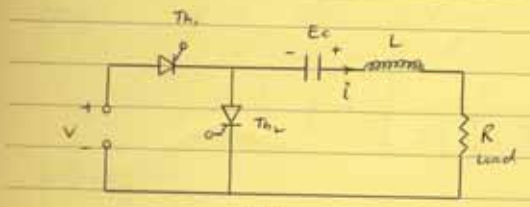
* It's a dc to ac converter.
* The o/p voltage and freq can be variad as per requirement of load.
* i/p may be from a battery, a solar cell or fuel cell.
* Utilization:
  - Domestic application.
  - Commercial installation as a source of standby power.
  - Variable speed ac drivers.
  - Induction heating.
  - HVDC power transmission.

Classification

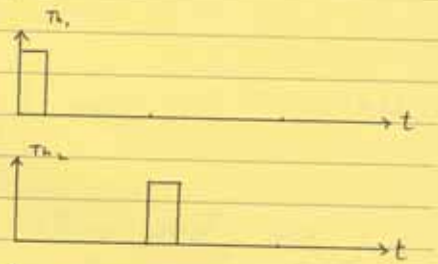
* With respect to:
  (1) Single or 3 ϕ
  (2) Naturally commutated or forced commutated.
  (3) The connections of thyr viz: series, parallel or bridge.

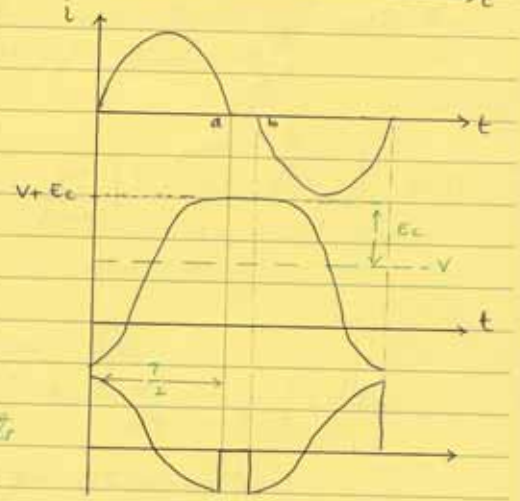
Date 03.04.2008

Series Inverter



(a)





Modes of Operation

- Mode 1 : Th_1 on.
- Mode 2 : Th_1 & Th_2 both off.
- Mode 3 : Th_2 ON.

* Series inv is so called due to commutating elements in series with load.
* Due to LC tank cap is charged at V+Ec and continues to charge in opposite polarity.

$$R^2 < 4L/C$$

* Drawbacks: ckt can't operated without Mode-2. Can't turn ON both SCRs at a time.

Date 03.04.2008

The above sequence is modes is repeated in next cycle when Th_1 is turned ON. The freq of o/p voltage is:

$$f = \left[\frac{1}{2\left(\frac{T}{2} + T_{off}\right)}\right] \text{ Hz} \qquad \ldots (4.2)$$

where,

$\frac{T}{2}$:= Time period of oscillation and T_{off} is time gap b/w turn off one thyr and turn ON of 2nd thyr.

Also,

$$\frac{T}{2} = \frac{\pi}{\left(\frac{1}{LC} - \frac{R^2}{4L^2}\right)^{0.5}} = \frac{\pi}{\sqrt{\omega_r}} \qquad \ldots (4.3)$$

(b) Analysis:

When Th_1 is turned ON, KVL

$$V + E_c = Ri + L\frac{di}{dt} + \frac{1}{C}\int i\,dt$$

where

E_c is initial voltage across cap.

Taking Laplace transform:

$$\frac{V}{s} + \frac{E_c}{s} = I(s)\left[R + sL + \frac{1}{Cs}\right] \qquad \ldots (4.5)$$

Since ckt is underdamped solution for (4.5) is

$$i = \frac{V + E_c}{\omega_r L} e^{-\frac{Rt}{2L}} \sin(\omega_r t) \qquad \ldots (4.6)$$

where

$$\omega_r = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \quad \text{(rad)}$$

Date 03.04.2008

Drawbacks

1.— The max possible freq is limited to damped freq of osc^n i.e $\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$. This is due to fact that Th_1 must be turned off before Th_2 is turned ON. Otherwise the supply voltage 'V' will be short ckt'd.

2.— When freq is less than damped freq distortion of o/p voltage waveform is high b/c T_{off} is large in comparison with ON time.

3.— The ckt component carry load I continously. The cap supplies load I in every -ve h.c Thus 'I' rating of commutating elements L and C are high.

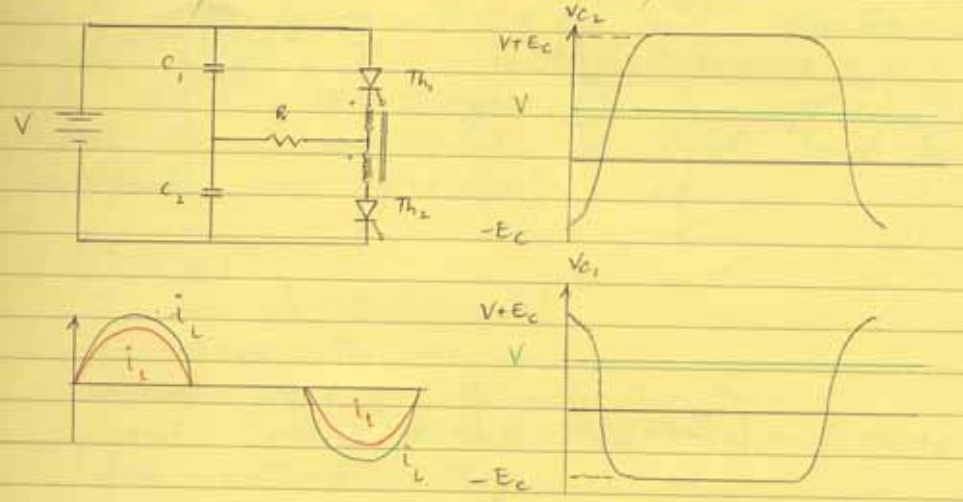
4.— The source supplies load intermittently (only during +ve h.c). Therefore, source should have a high 'I' rating also. Source current has high Harmonic content.

5.— Max load 'I' current depends on load resistance. Therefore output regulation of inverter is poor.

Date 09.04.2008

Modified Series Inverter

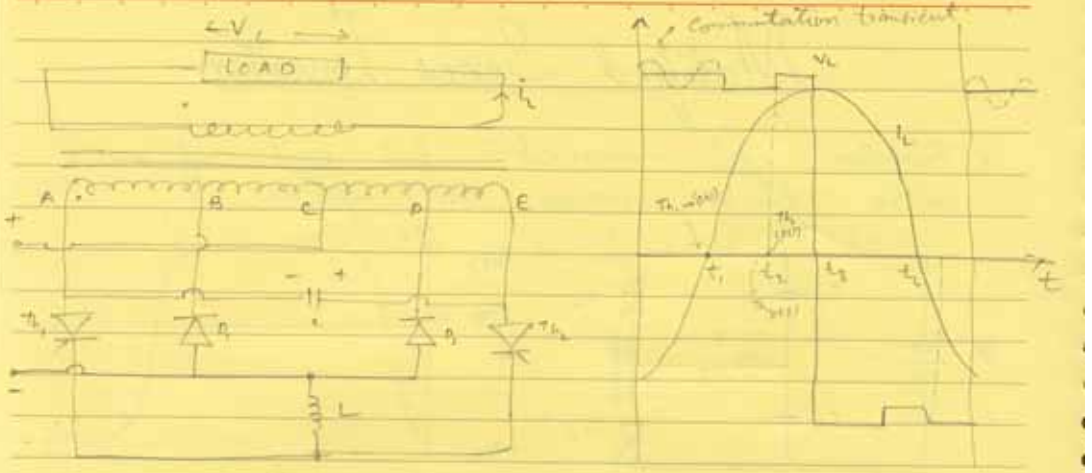
* Problem is removed but cost of extra power ~~conver~~ consumption.



Parallel Inverter

Page 93

Date



(Parallel Inverter)

(PARALLEL Inverter)

Date 09.04.08

- Cap and load are effectively in parallel

MODE 1:

- Th_1 turned ON at t_1.
- Battery current flows thru C-A-Th_1-L.
- No of turns CA, EC and secondary are equal. Thus voltage B/w E & A is 2V (if V is i/p to 11-inverter).
- Due to 'L' nature of load, load current inc gradually.

MODE 2:

- Th_2 is ON at t_2
- C turns Th_1 OFF.
- Current flows: Th_2 – L – D_1 – B – A
- Load voltage will be +ve and more than battery voltage.
- i_L will flow thru CB and diode D_1 to -ve of battery b/c D_1 is fwd bias and cap discharge current is more than load current.
- Potential at B raises sufficiently to rev bias D_1.
- The Cap discharge thru Th_2 will stop
- Now inductor current will take path: L – D_2 – DE – Th_2 will during this. D is connected to -ve of battery hence polarity of VL will rev and cap will be charged to slightly more than 2V now in opposite direction.

Date 09.04.2008

- Th_2 will stop when 'i' current becomes zero thru it.

MODE 3:

- when i_L will = 0, D_2 stops conducting.
- Then at t_4 the Th_1 is triggered ON again to reverse the direction of current thru load.
- During t_4 to t_5 load voltage V_L and load current i_L are reversed.
- At t_5, Th_1 is triggered ON again.

Some Observations:

* Each of thyr turns ON twice during each half cycle.
* Interval t_2 to t_4 is load dependent.
* Thus each thyr has to be gated by a pulse train for a minimum duration of $\frac{1}{4}$ cycle.
* Feed back diode conducts during t_2 to t_4, and during this period load voltage will be more than V.

Control of output Voltage

* The o/p voltage can be controlled from dc side or from ac side.
* In control from dc side, i/p dc

Date 10.4.08

voltage is varied and this changes o/p rms voltage.

* Variable i/p voltage can be obtained either from a controlled rectifier or from a chopper circuit.
* Chopper circuit introduces greater harmonics thru.

* Control from ac side would include a transformer mostly with multiple tapping

Design of Commutation elements 'L' & 'C':

The diode D_1 will conduct till current reaches peak value.

when D_1 conducts, Th_1 is rev biased this time must be allowed equal to turn off time of SCR.

$$t_q = \frac{\pi}{3}\sqrt{LC}$$

Also reflected load current at secondary of tr/r is given by

$$\hat{I}_L = V\sqrt{\frac{C}{L}}$$

Date

Example 4.4: A parallel inverter has i/p dc voltage of 40 V. It is desired that o/p voltage to be 230 V, 50 Hz and peak load current 2A. Design parallel inverter, chose correct ratings of SCR

Sol

Let Turn off time = 50 μsec

load current $i_L = 2A$

Since i/p is 40 V & o/p is 230 V

Reflected load current is given by

$$i_L' \times 40 = 2 \times 230$$

$$i_L' = \frac{460}{40}$$

$$i_L' = 11.5 \text{ A}$$

Now using eq 4.10 & 4.11

$$t_q = \frac{\pi}{3}\sqrt{LC}$$

$$50 \times 10^{-6} = \frac{\pi}{3}\sqrt{LC}$$

$$\frac{\pi^2}{9} LC = 50 \times 10^{-12}$$

And

$$i_L = V\sqrt{\frac{C}{L}}$$

So

$$L = 166.04\ \mu H$$

$$C = 13.73\ \mu F$$

Date 10-04-2008

The reflected load current is 11.5 A, allowing a margin of about 1.5 SCR current rating is 20 A. Voltage rating of 100 V is suitable.

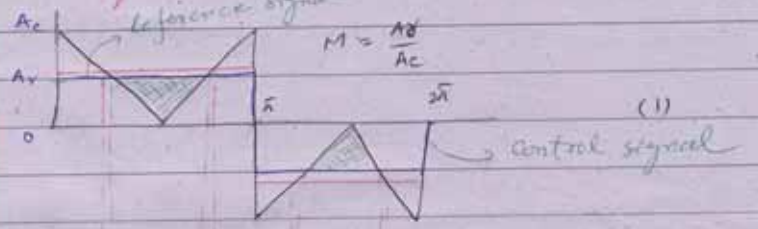
Therefore, a voltage rating of 100 V is suitable with 20 A of current and 50 μsec to turn-off time.

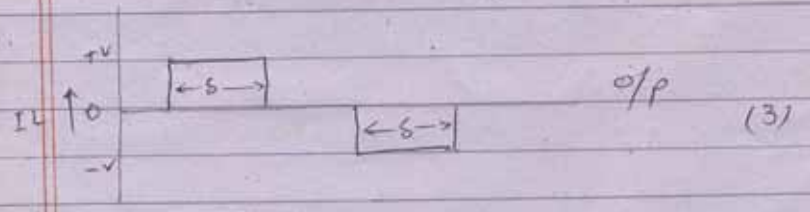
16.04.08

Power Electronics

PWM Techniques

They come under fundamental techniques.





* o/p generated depending upon decision makers in waveform-1.
* If in waveform-1 reference voltage is not the o/p pulse width will change.

* The rms value o/p voltage is

$$V_L = \left[\frac{2}{2\pi} \int_{\frac{\pi-\delta}{2}}^{\frac{\pi+\delta}{2}} V^2 d(\omega t) \right]^{0.5} = V\sqrt{\frac{\delta}{\pi}} \qquad (4.16)$$

where V is i/p voltage.

The fourier series o/p voltage is

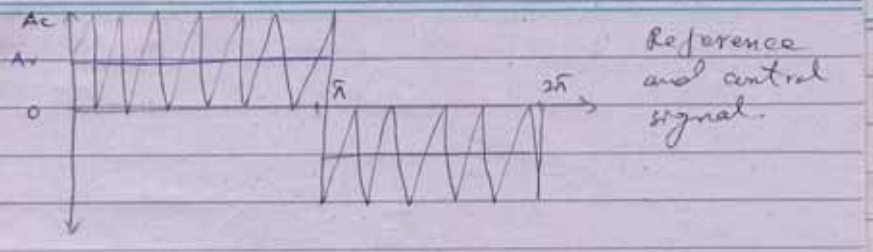
$$V_L(t) = \sum_{n=1,3,5}^{\infty} \frac{4V}{n\pi} \sin\frac{n\delta}{2} \sin(n\omega t) \qquad (4.17)$$

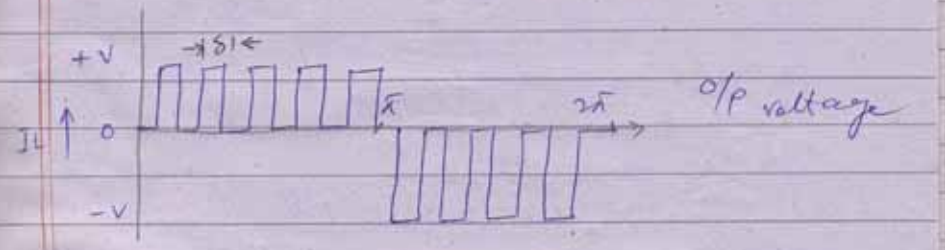
* The even harmonics are absent in waveform as a symmetrical waveform is resulted.

Multiple PWM

(5)

* Single PWM technique has higher harmonic content in o/p waveform.
* The harmonic content can be reduced by having many pulses in each half cycle of o/p.
* If higher harmonics lower the fundamental content. (lo





The freq of reference signal A_r control frequency of o/p. The carrier signal is a triangular wave having a frequency (f_c). Freq (f_c) determines number of pulses in each half cycle. The ratio $\frac{f_c}{f_o}$ is known frequency modulation ratio (f_o = freq of o/p). The no. of pulses in each half cycle is:

$$P = \frac{f_c}{2f_o} = \frac{m_f}{2} \qquad (4.18)$$

where 'P' = no. of pulse in each h.cy and m_f = freq modulation ratio.

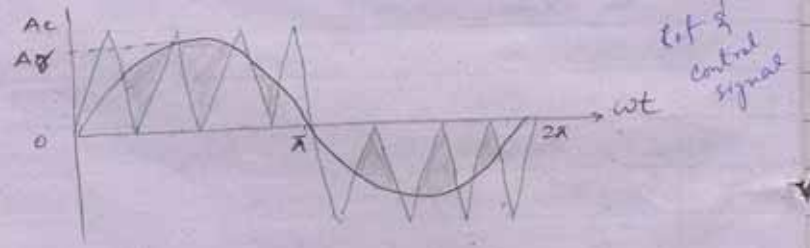
The variation of ratio $\left(\frac{A_r}{A_c}\right)$ 0 to 1 changes pulse width from 0 to $\frac{\pi}{P}$ and o/p voltage from 0 to V. P width of each pulse the rms value of o/p is:

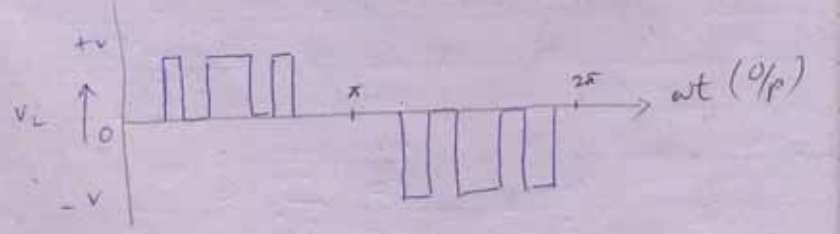
$$V_L = \left[\frac{2P}{2\pi} \int_{\frac{\pi}{P} - \frac{\delta}{2}}^{\frac{\pi}{P} + \frac{\delta}{2}} V^2 \, d(\omega t) \right]^{0.5}$$

$$V_L = V\sqrt{\frac{P\delta}{\pi}} \qquad (4.19)$$

(17,04,08) Slide # 10

Sinusoidal PWM





Extract info from Web on ~~HV~~ High Voltage DC transmission, the report would be based on operational methods, merits and limitation. The report will be in Own words should not exceed 4-A4 Pages (2 Pages-back to back) All diagrams / sketches for explanation would be drawn in freehand. (Next Wednesday) (Assignment # 2)

(in PWM)

* The reference signal is a sinusoidal wave.
* The control sig is a triangular wave frequency fc
* Sinusoidal sig's frequency controls frequency of o/p voltage of inverter.
* The peak value Ar of reference sig controls modulation index.
* The carrier and reference waves are mixed in a comparator.
* When magnitude of reference signal is more than that of carrier signal then o/p of comparator is high and pulse is generated.
* This pulse triggers SCR into conduction and a voltage o/p occurs.

(103)

* The widths of o/p pulses are not same.
* Width depends upon angular position of pulse.
* Width is direct fn of angle.
* By varying modulation index, we can vary rms value of o/p waveform.
* If δ_m, width of m^{th} pulse the rms value of o/p voltage is

$$V_L = V \left[\sum_{m=1}^{p} \frac{\delta_m}{\pi} \right]^{0.5} \qquad (3.20)$$

where 'p' is no. of pulses on one half cycle of o/p waveform.

Ex 4.13

(Example: 4.13) A single ϕ full bridge inverter has purely resistive load and its voltage is controlled by multiple pulse width modulation technique. The width of each pulse is 30° and each half cycle has 5 pulses. If voltage 200V. find (a) rms value of o/p. (b) pulse width to maintain o/p power constant if i/p voltage inc by 10% (c) Maximum possible i/p voltage if max possible pulse is 33°.

(104)

(17,04,08)

4.13

(a) $V_L = 200\sqrt{\frac{5\times 30^\circ}{180}}$

$V_L = 182.57\ V$

(b) Input voltage = $200 \times 10\% = 20$

$= 220\ V$

$182.57 = 220\sqrt{\frac{5\times\delta}{180}}$

$\sqrt{\frac{5\times\delta}{180}} = \frac{182.57}{220}$

$\frac{5\times\delta}{180} = (0.8298)^2$

$\frac{5\times\delta}{180} = 0.6886$

$\delta = 24.79^\circ$

(c) $182.57 = V\sqrt{\frac{5\times 33^\circ}{181^\circ}}$

$V = 190.65\ V$

(Ex: 4.14) A single ϕ full wave inverter is fed by 200V DC source. The o/p voltage is controlled single pulse. The reference signal is more than for 120° in each half cycle. Find rms value of o/p?

with $\delta = 120^\circ$

eq (4.16)

$V_L = 200\sqrt{\frac{120}{180}}$

$V_L = 163.3\ V$

(Ex: 4.15) A single ϕ inverter is controlled by Sinusoidal PWM. The I/p volts is 150. The ref and control ckts are so adjusted that ref signal is more than signal from 20° to 40°, 60°–120°, 140°–160° in each half cycle. Find rms o/p

There are 3 pulses in each hyperbola

The width of first pulse 20°, 2nd = 3rd = 20°

using eq (4.20)

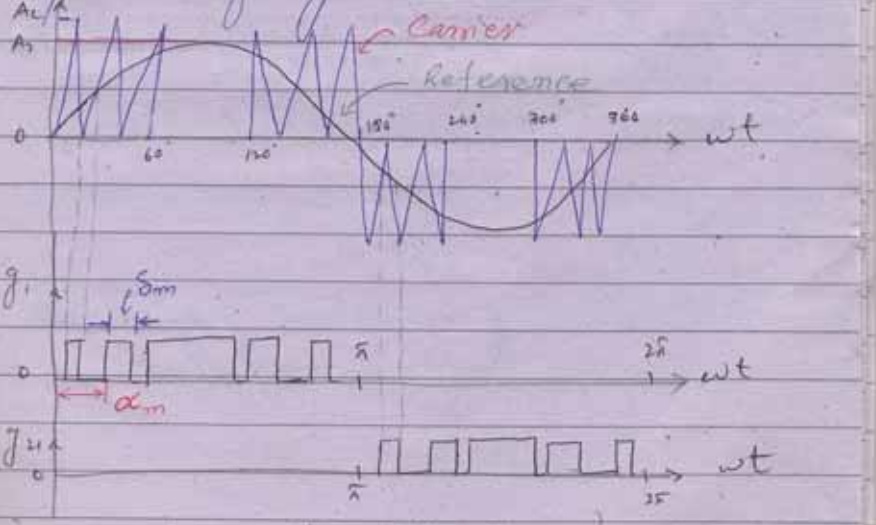
$V_L = 150\left[\frac{20}{180} + \frac{60}{180} + \frac{20}{180}\right]^{0.5}$

$V_L = 111.80\ V$

(17,04,08)

Modified PWM (Slide #11)

* The width of pulse near peak of sine wave doesn't vary with variation of modn index.
* This is due to property of sine wave and based upon it Sinusoidal pwm technique can be modified.
* In modified sinusoidal pulse w.m. (MSPWM) technique, carrier wave is applied during first and last 60° intervals per half cycle.

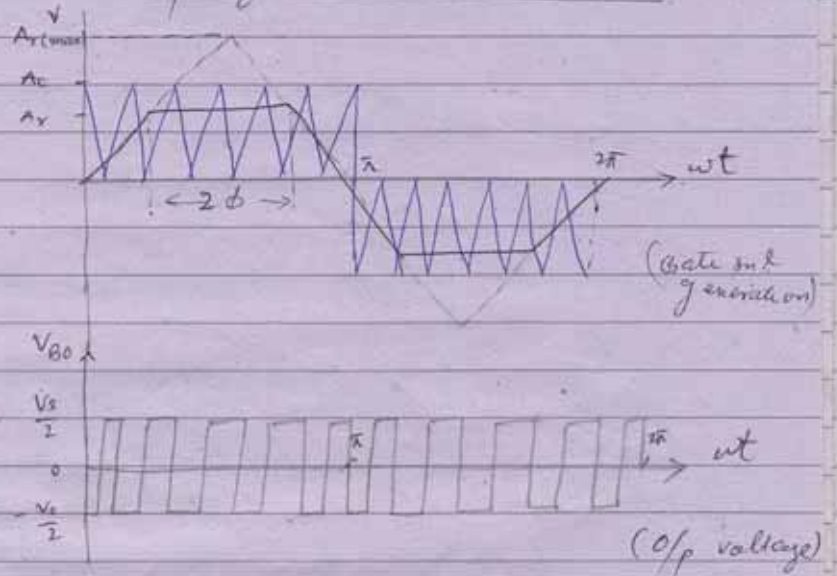


* Advantages of this technique:
  - Fundamental component is inc↑ and its harmonic characteristics are improved.
  - It reduces no. of switching of power devices and also reduces switching losses.

Advanced modulation Techniques

* The sinusoidal pulse w.mod technique suffers from draw back of lower fundamental level.
* The following are other modulation techniques that offers improved performance:
  (1) Trapezoidal.
  (2) Staircase.
  (3) Stepped.
  (4) Harmonic injection.
  (5) Delta modulation.

(1) Trapezoidal Modulation



* A triangular wave is compared with a modulating trapezoidal wave.

* The trapezoidal wave can be obtained from triangular wave by limiting its magnitude to $\pm A_r$, which is related to peak value $A_{r(max)}$ by

$$A_r = \delta A_{r(max)}$$

where 'δ' is called triangular factor, the waveform becomes a Δ wave

when $\delta = 1$, the mod index M is

$$M = \frac{A_r}{A_c} = \delta \frac{A_{r(max)}}{A_c}$$

for $0 \le M \le 1$ (6.48)

* The angle of flat portion of trapezoidal wave is given by,

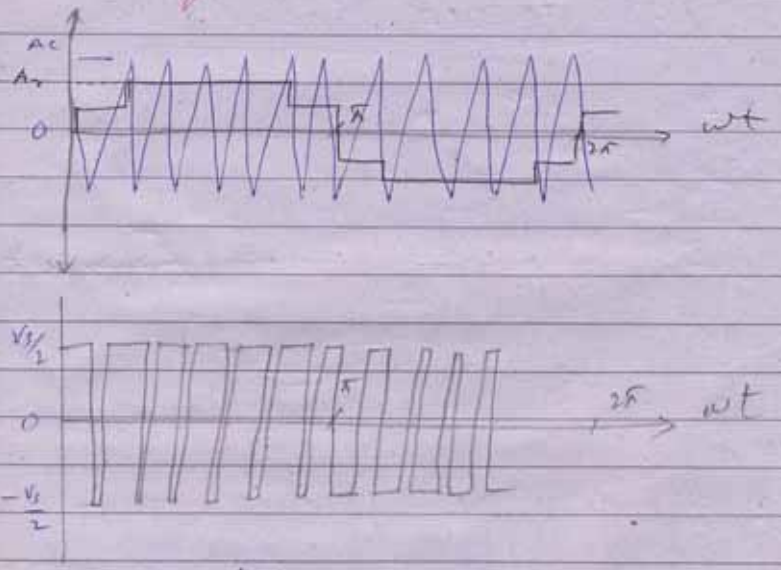
$$2\phi = (1 - \delta)\pi \qquad (6.49)$$

* For fixed values of $A_{r(max)}$ and A_c, M that varies with o/p voltage can be varied by changing triangl factor (δ). This type of modn ing peak fundamental o/p voltage upto 1.05 V_s, but o/p contain Lower order harmonics (LOHs).

(17,04,08)

(2) Staircase Modulation

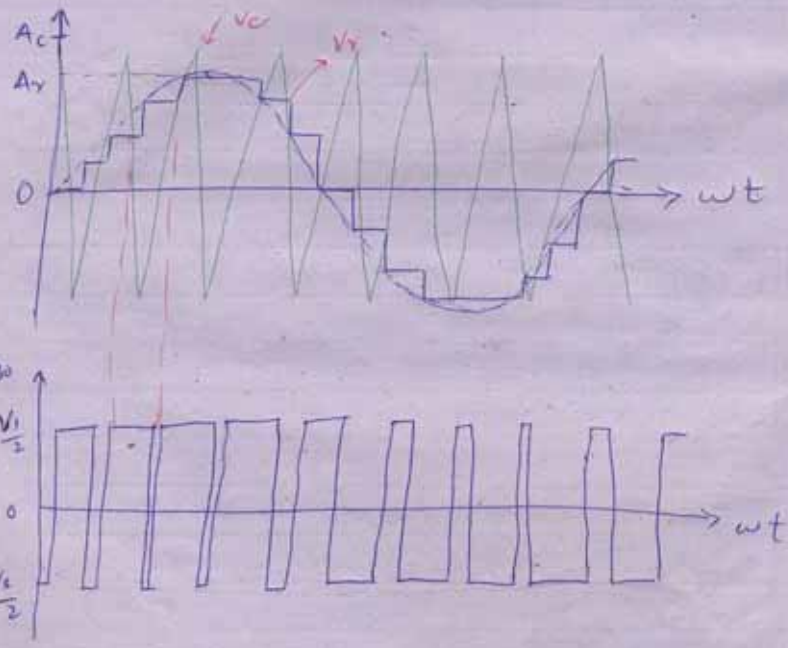
* In this technique you can pick a specific harmonic point and change variate it accordingly to requirement.



* The staircase is not a sampled approximation to sine wave rather the levels of stair are calculated to eliminate certain harmonics.
* The modn freq (m_f) and no of steps are chosen to obtain desired quality of o/p voltage
* Not recommended for fewer than pulses in 1 cycle.
* With this method high quality having fundamental value of upto $0.94 V_s$ can be achieved.

23,04,

(3) Stepped Modulation



* Uniform steps.
* Not approximation of sine wave

(23,04,08)

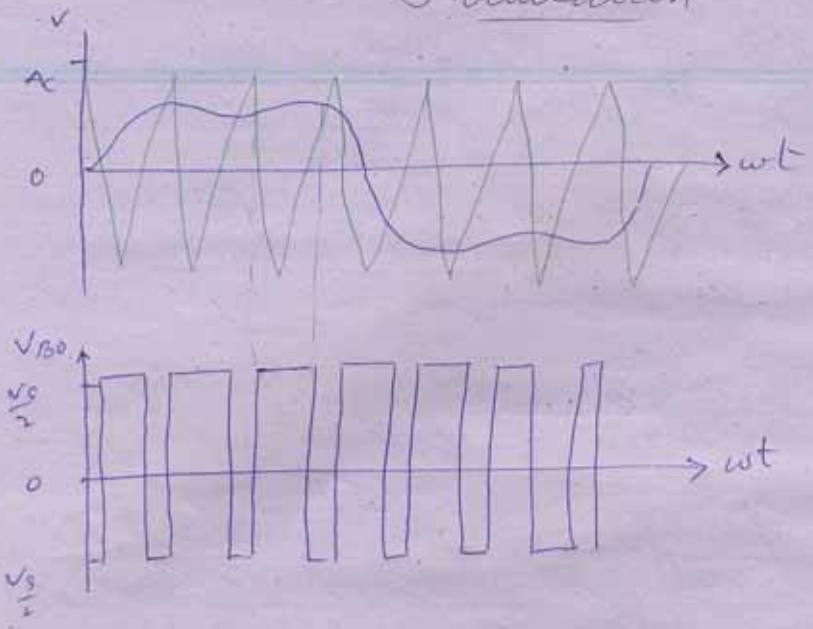
* Modulating signal is stepped wave as shown in figure.
* It is not a sampled approximation to the sine wave rather it is divided into steps say 20° with each interval.
* Tair control specific harmonic contents to control specific harmonic contents to control fundamental and even can eliminate certain harmonics.
* Such type of PWM gives higher fundamental amplitude with low distortion.

Control elements:

(1) No. of pulse
(2) Step length (3) Step height.

(2) to control fundamental, to suppress power of harmonics, to target specific harmonic content.

(4) Harmonic Injection Modulation



* The modulating signal is generated by injecting selected harmonics to sine wave.
* As a result of that, a flat-topped waveform is generated that reduces amount of over-modulation.
* It provides a higher fundamental amplitude with lesser distortion.

Generally modulating signal is composed of:

(6.50) $V_r = 1.15 \sin\omega t + 0.27 \sin 3\omega t - 0.029 \sin 9\omega t$

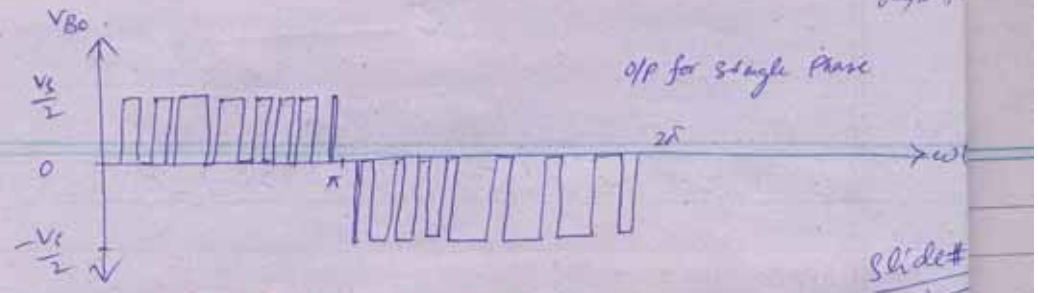
Injection of 3rd harmonics does not effect quality of output voltage, b/c o/p of a 3φ inverter does not contain triplen harmonics.

If only 3rd harmonic is injected the modulating signal is given by

$V_{r(mod)} = 1.15 \sin\omega t + 0.19 \sin 3\omega t$ (6.51)

The signal can be generated by $2\pi/3$ segments of a sine wave as shown.

Q Draw the modulating signal waveform for a harmonic injection modulation when freq of fundamental is 50Hz?



o/p for single phase

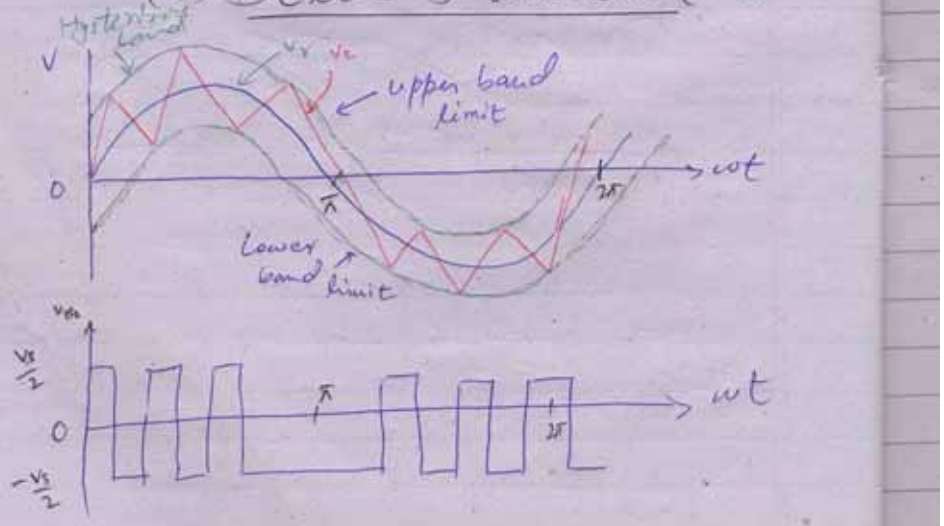
Slide#

Features of this PWM:

- The line-to-line voltage is sinusoidal form and amplitude of fundamental component is approximately 15% more than that of a normal sinusoidal PW
- As obvious, each arm is switched off for 1/3rd of period, heating of switching devices is reduced.

24.04.

(5) Delta Modulation



24,04,08

* Basic of delta modulation → specialized triangular wave form.

* A triangular wave is allowed to oscillate within a defined window δV above and below reference sine wave V_r.
* The modulation is also called hysteresis modulation.
* Change in modulating sine freq (keeping slope of Δ wave constant) would result in change in the pulse width and no. of pulses.

hysteresis: ⊛ Quality of a system to retain its original position.
⊛ Depends on amount of current, and core material.

* If hysteris of inverter is large inverter is lossy.
* To change o/p simply change frequency of Carrier signal.

(*) The fundamental o/p voltage can be upto $1V_s$ and is dependent on peak amplitude A_r and freq f_r of reference signal.

(*) The delta modn. can control ratio voltage to freq, which is utilized in ac motor speed control.

(24,04,08)

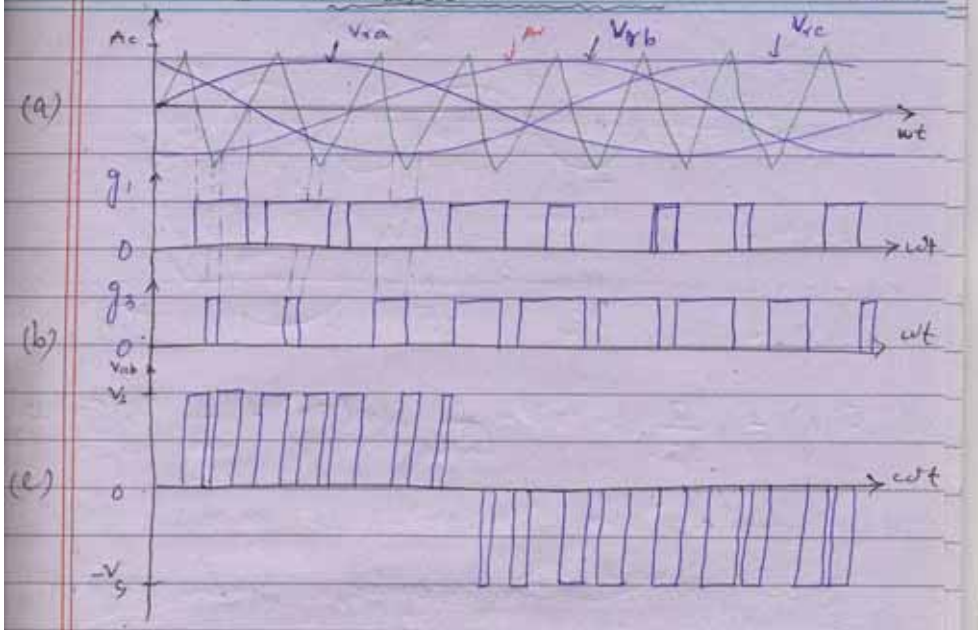
Voltage Control of 3ϕ Converter

(*) A 3ϕ inverter can be thought as 3 single converters operating in parallel.

(*) with this analogy, all previous techniques can be utilized to control o/p voltage of 3ϕ converter, however following are most common techniques for o/p voltage control of 3ϕ converter.

1- Sinusoidal PWM.
2- 3rd Harmonic PWM.
3- 60° PWM.

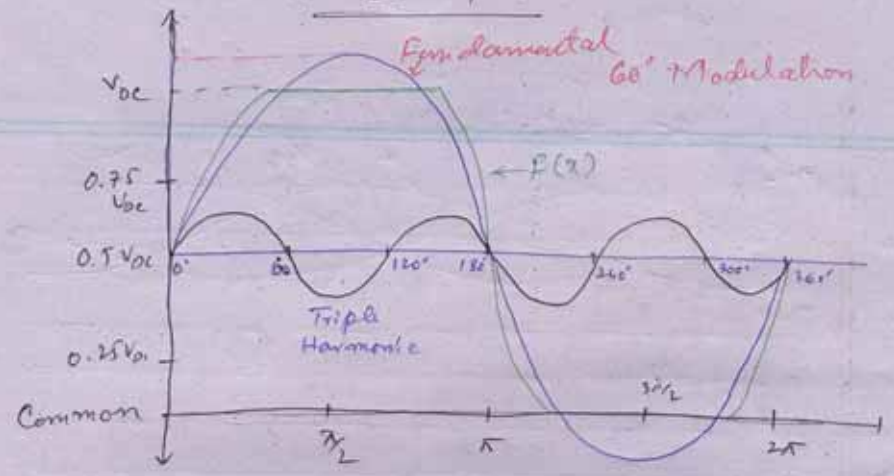
1- Sinusoidal PWM (3:19)



The peak amplitude of line o/p voltage is given by

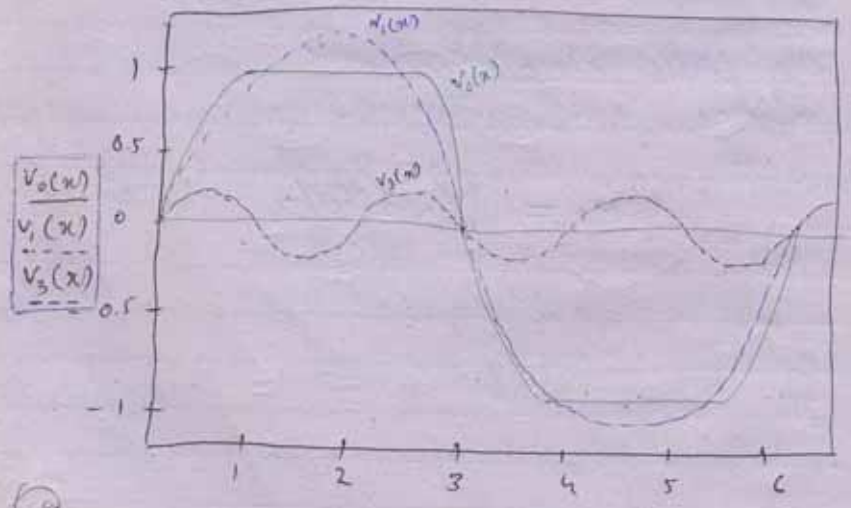
$$V_{ab_1} = M\sqrt{3}\,V_s/2 \quad \text{for } 0 \le M \le 1$$

2- 60° PWM



$$F(x) = \frac{2}{\sqrt{3}}\sin(x) + \frac{1}{2\pi}\sin(3x) + \frac{1}{60\pi}\sin(9x) + \frac{1}{280\pi}$$

* modulating signal containing fundamental and 3rd harmonic component multip



(24-04-08)
(9:24)

2. 60° PWM

- 60° PWM is similar to modified PWM
- The idea is to make modulating signal flat top from 60° to 120° and flat from 240° to 300°.
- The power devices are held on for one-3rd of cycle and thus have reduced switching losses.
- All triple harmonics are absent in 3ϕ voltages.

- 60° PWM creates a larger fundamental $\frac{2}{\sqrt{3}}$ and utilizes more of available dc voltages.
- Phase voltage : $V_p = \frac{0.57735}{V_s}$

and line voltage : $V_L = V_s$

Draw the wave form of modulating signal for a 3ϕ, 60° pwm system operating at a fundamental freq of 50Hz ?

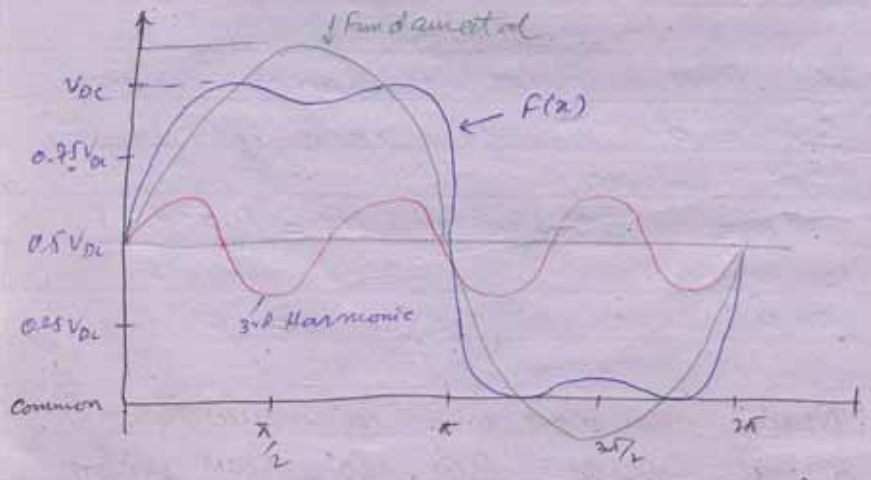
$f = 50Hz$

$f(0)=0$, $f(30°)=71.24$, $f(60°)=1$, $f(90°)=-69.51$
$f(120°)=1$, $f(150)=71.24$, $f(180)=0$, $f(210)=-71.24$

$f(240)=-1$, $f(270°)=69.51$
$f(300°)=-1$, $f(330)=-71.24$
$f(360°)=0$

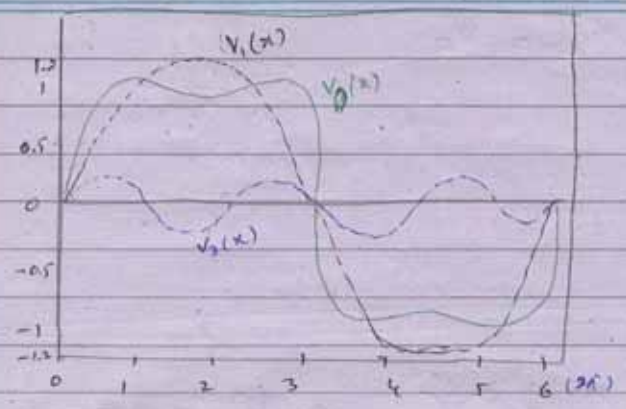
(30°) (60°) (90°)
$f(0)=0$, 0.731, 1, 1, 1, 0.731, 0.501, 210, -0.731

(3) 3ϕ Harmonic PWM



$$F(x) = \frac{2}{\sqrt{3}}\sin(x) + \frac{1}{3\sqrt{3}}\sin(3x)$$

26-04-08



* 3rd harmonic PWM is similar to selected harmonic injection method.
* The diff is that reference Ac waveform is not sinusoidal but consist of both a fundamental component and a 3rd harmonic component.
* As a result peak-peak amplitude of ref fns does not exceed DC supply V_s.
* But fundamental component is higher than supply.
* 3rd harmonics are cancelled out in ~~ratio~~ neutral as before.
* $V_p = V_s/\sqrt{3} = 0.57735\ V_s$
* The fundamental component peak amplitude $V_{p1} = 0.57735 V_s$ and peak voltage is $V_L = \sqrt{3} V_p = \sqrt{3}(0.57735 V_s)$

  So $V_L = V_s$
* This is 15.5% higher in amplitude than sinusoidal PWM.

02,05

DC-DC CONVERTER

(CHOPPERS)

* Industrial applications often require fixed DC voltage to be converted into variable DC voltage.
* DC-DC converter performs that operation.
* It is equivalent to trfr in AC.
* Buck & boost operations are possible.
* Buck - Step down
* Boost - Step up

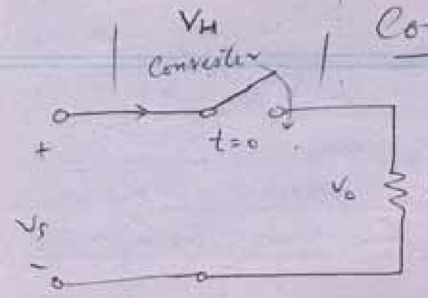
Buck-boost → variable step down or up

02,05,08

* Typical Applications include:
* Traction motor control in electric trolly, automobile, marine, hoists forklift truck and mine haulers.
*
* Properties: Smooth accelration control high η and fast dynamic response.
* They can be used in re-generative braking of DC - motor.
* This returns back energy to supply and this saves energy for transportation system for frequent stops. ↳ e.g Automobile industry: Conveir belt.
* DC convts are used in voltage regulators with inductor to make constant current source.

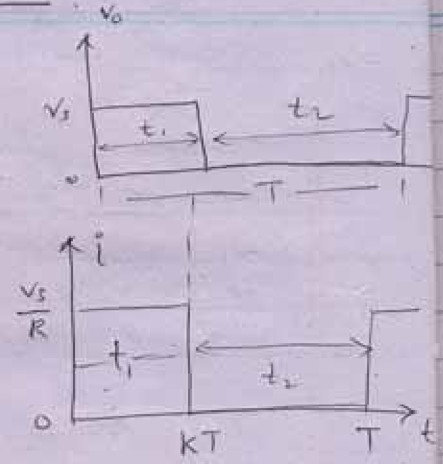
Step down DC - DC Converter

(7) 02,



S.1(a)

↳ Very very basic type of buck converter.



S.1(b)

* As there is turn-off time is present so A7 O/p < I/p (Basic Theory)
* V_H := Voltage drop of switching device.
* The average o/p is given by

$$V_a = \frac{1}{T}\int_0^{t_1} v_0\,dt = \frac{t_1}{T} V_s = f t_1 V_s$$

$$V_a = k V_s$$

and average load current

$$I_a = V_a/R = kV_s/R$$

(02,05,03)

~~and avg load~~

where

'T' is chopping period

'k' = t_1/T is duty cycle

chopper

'f' is chopping frequency.

* Rms value of o/p is

$$V_0 = \left(\frac{1}{T}\int_0^{kT} v_0^2\, dt\right)^{1/2}$$

$$V_0 = \sqrt{k}\, V_s \qquad (5.2)$$

* Assuming a loss less converter, i/p power to converter is as o/p power and given by:

$$P_i = \frac{1}{T}\int_0^{kT} v_0 i\, dt = \frac{1}{T}\int_0^{kT} \frac{v_0^2}{R}\, dt$$

$$P_i = k\,\frac{V_s^2}{R} \qquad (5.3)$$

Effective i/p resistance seen by same source is;

$$R_i = \frac{V_s}{I_a} = \frac{V_s}{kV_s/R} = \frac{R}{k} \qquad (5.4)$$

* This means that converter makes i/p resistance R_i as a variable resistance R/k.

* I/p resistance is fn of duty cycle:

$$R_i = \frac{R}{k} = \frac{R}{t_1/T} \qquad (10)$$

* Duty cycle 'k' can varied by:
  - ↳ varying t_1, T or f.

* o/p voltage thus can be varied from 0 to V_s.

* Constant freq. Operation:

f and thus T is kept constant, the ON time t_1 is varied, PWidth thus varies, thus it calls PWM Control.

* Variable freq oper.

(02,05,08)

Variable freq Operation: (11)

Switching frequency f is varied, either on or off time is kept constant called FM large freq variation is required for complete control of o/p voltage.

This would generate harmonics at unpredictable freq and filter design would be difficult.

Finding Performances of a DC-DC converter. (12)

The dc converter in fig 5.1a has R = 10Ω i/p voltage V_s = 220V when converter remains ON V_{CH} = 2V and chopping freq f = 1kHz duty cycle 50%. Determine (a) Avg o/p V (b) Rms o/p V_0 (c) η (d) R_i (e) Rms of fundamental component of o/p harmonic voltage.

eq (5.1) $V_a = kV_s \Rightarrow 0.5 \times (220-2) = 109$ V

eq (5.2) $V_0 = \sqrt{k}\,V_s \Rightarrow \sqrt{0.5} \times (220-2) = 156.15$ V

(c) $$P_0 = k\left(\frac{V_s - V_{CH}}{R}\right)^2 \quad \text{— (5.5)}$$

$$= \frac{(0.5)\,(220-2)^2}{10}$$

$$P_0 = 2376.2\ W$$

* i/p can found from

$$P_i = k\,\frac{V_s\,(V_s - V_{ch})}{R} \quad \text{— (5.6)}$$

$$= \frac{(0.5)\,(220)\,(220-2)}{10}$$

$$P_i = 2398\ W$$

$$\eta = \frac{P_0}{P_i} = \frac{2376.2}{2398} = 99\%$$

(d) eq (5.4) $R_i = \frac{R}{k} = \frac{10}{0.5} = 20\Omega$

(e) o/p voltage can express in Fourier series as

(o/p) $$V_o(t) = kV_s + \frac{V_s}{n\pi}\sum_{n=1}^{\infty} \sin 2n\pi k \cos 2n\pi ft + \frac{V_s}{n\pi}\sum_{n=1}^{\infty}(1-\cos 2n\pi k)\sin 2n\pi ft \quad (5.7)$$

The fundamental component (n=1) o/p voltage can be eq (5.7)

$$V_1(t) = \frac{V_s}{\pi}\left[\sin 2\pi k \cos 2\pi ft + (1-\cos 2\pi k)\sin 2\pi ft\right] \quad \hookrightarrow (5.8)$$

$$= \frac{220\times 2}{\pi}\sin(2\pi \times 1000t)$$

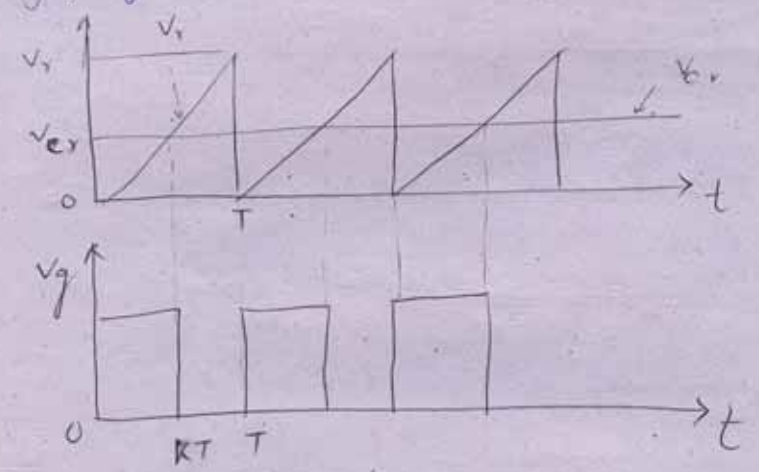
$$= 140.06 \sin(6283.2t)$$

and its rms $V_1 = 140.06/\sqrt{2}$

$V_1 = 99.04$ V.

Duty Cycle Generation (02,0

* By comparing a DC reference sig with a saw-tooth wave the duty cycle can be generated.



The reference sig is given by

$$V_r = \frac{V_r}{T}t \quad (5.9)$$

w/c must equal to carrier signal

$$V_{cr} = \frac{V_r}{T}kT$$

w/c give duty cycle k as

(32)

$$k = \frac{V_{cr}}{V_r} = M \quad (5.10)$$

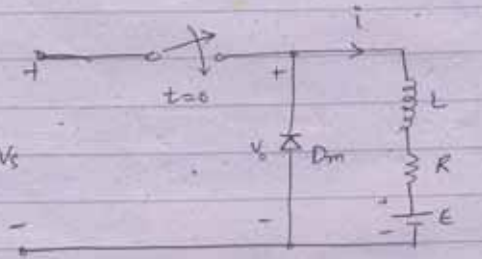
M := modulation index.

(02,05,08)

* By varying carrier s/l V_{cr} from $0 \to V_{cr}$ duty cycle 'k' can be varied from 0 to 1.

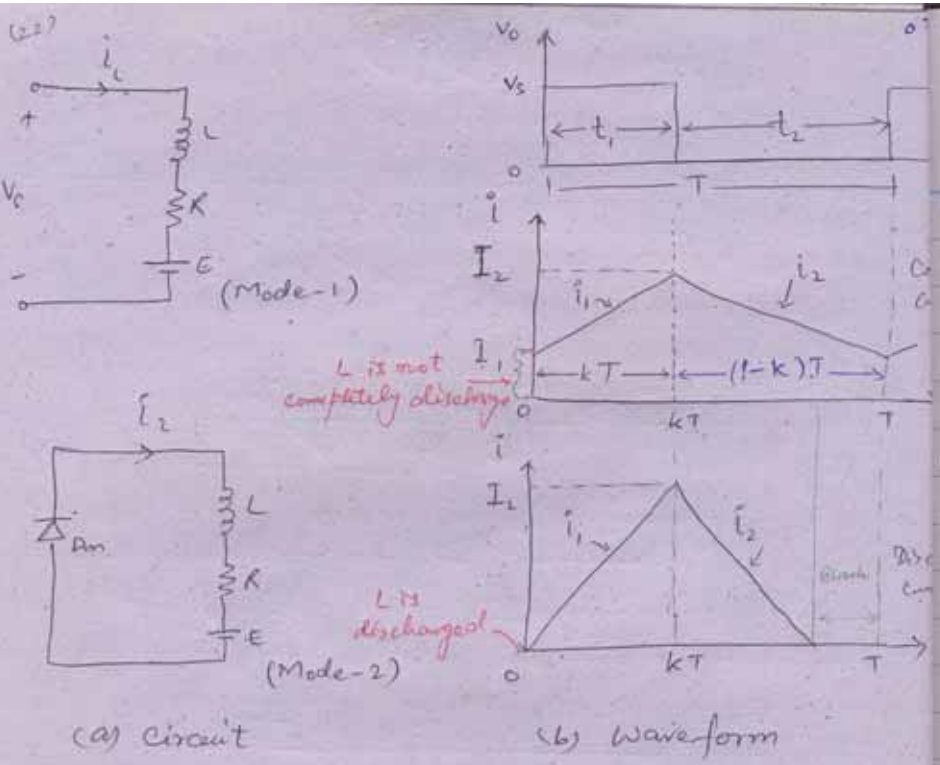
(19)
(20)

Step Down Converter with R-L load (07,05,08)



* Chopping is done by Switch.
* Two modes of operation
  (i) close switch (ii) Open switch.

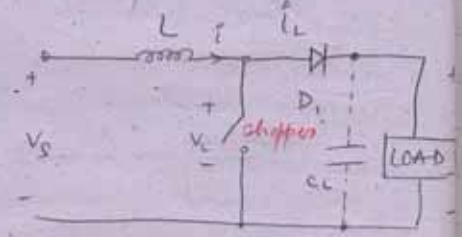
* Two mode of operation:
  - First mode: The converter is switched on, load current supplied thru supply.
  - 2nd mode: The converter is switched off, the load current is supplied thru free wheeling diode 'Dm'.
* This would happen as shown:



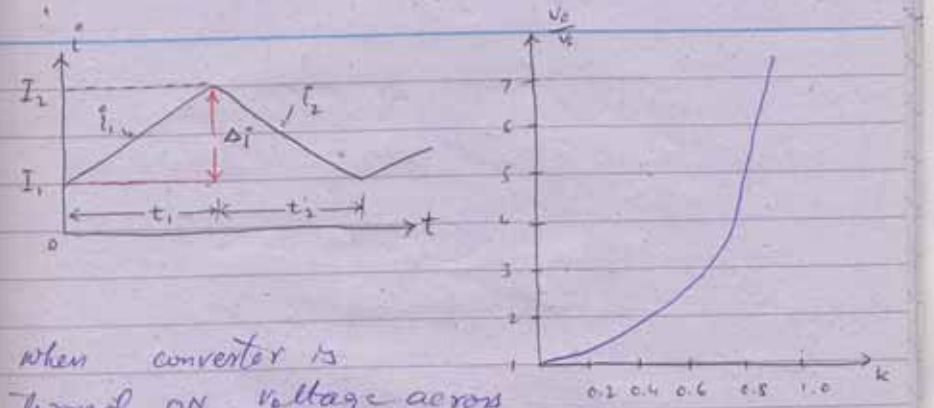
(23)

Step-up Operation

* L-C Tank circuit.



07,05,08



When converter is turned ON, voltage across 'L' is

$$V_L = L\frac{di}{dt}$$

and this gives p-p ripple current in 'L' as

$$\Delta I = \frac{V_s}{L} t_1 \qquad (5.26)$$

The average current is

$$V_o = V_s + L\frac{\Delta I}{t_2} = V_s\left(1 + \frac{t_1}{t_2}\right)$$

$$V_o = V_s \frac{1}{1-k} \qquad (5.27)$$

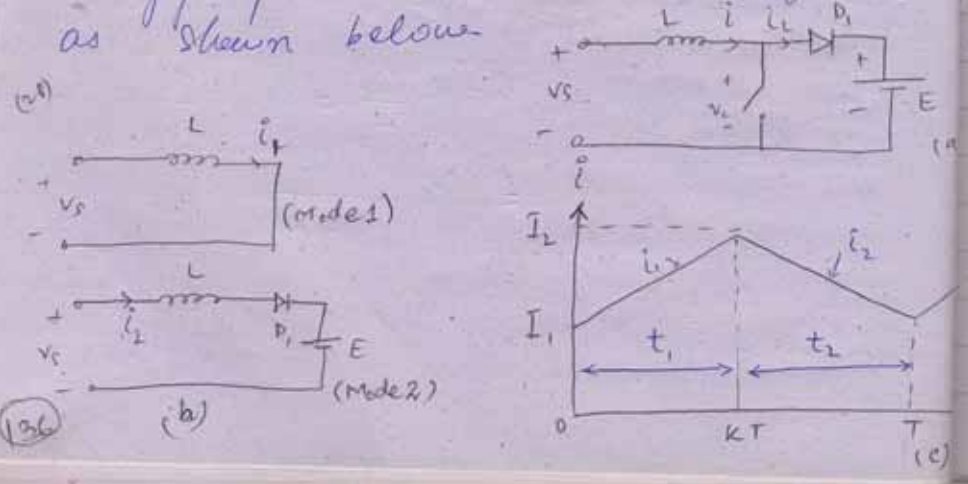
(26) Connecting a cap at o/p (as shown) would make o/p continuous and V_o would become average value 'V_a'.

As obvious from equation 5.27 we can vary o/p voltage and step it up, it by varying value of 'k'.

Min o/p voltage is 'V_s' when duty cycle ($k = 0$).

Making 'k' close to 1 would result in a high o/p as shown in diagram.

(27) This principle can be used to transfer energy from one source to other as shown below



08,05,08

* $V_s < E$:

- The presence of inductor,
- low voltage source can transfer power to high voltage source
  $\therefore V_s + V_L > E$
- E is absorbing power.

The inductor current for mode 1 is given by:

$$V_s = L \frac{di}{dt}$$

and expressed as

$$i_1(t) = \frac{V_s}{L} t + I_1 \qquad (5.28)$$

where I_1 is initial current for mode 1.
During mode 1, current must rise and necessary condition

$$\frac{di}{dt} > 0 \quad \text{or} \quad V_s > 0$$

The current for mode 2 is:

$$V_s = L \frac{di_2}{dt} + E$$

and solved as

$$i_2(t) = \frac{V_s - E}{L} t + I_2 \qquad (5$$

where I_2 is initial current for mode 2.
For stable system current must fall and condition.

$$\frac{di_2}{dt} < 0 \quad \text{or} \quad V_s < E$$

Stable system: A system free of oscillation

If condition is not satisfied, inductor current continous to rise and an unstable situation occurs.
Therefore, the condition for controllable power transfer as;

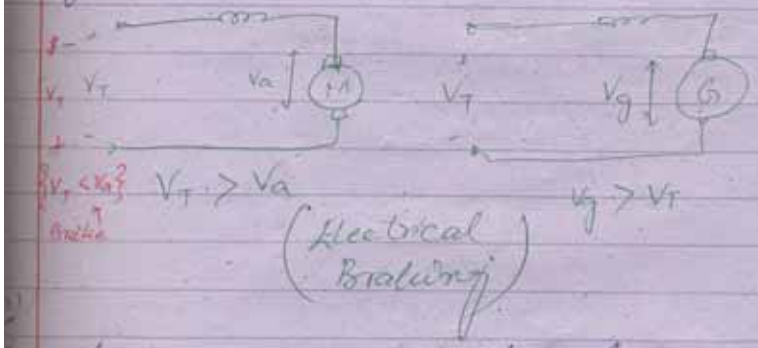
$$0 < V_s < E \qquad (5.30)$$

Controllable power is only for stable systems.

For transferring power from a fixed (or variable) source to fixed dc voltage by (5.30) must be observed.

08,05,08

* In electrical braking of dc motors where motors behaves as a generator, the terminal voltages falls when machine's speed elect, converter permits power transfer to a fixed dc source or a rheostat.



When converter is turned on, energy is transferred from source 'V_s' to inductor. If converter is off, a magnitude of energy stored in inductor is forced to battery 'E'.

Without chopping action, V_s must be greater than 'E' for transforming power from V_s to E.

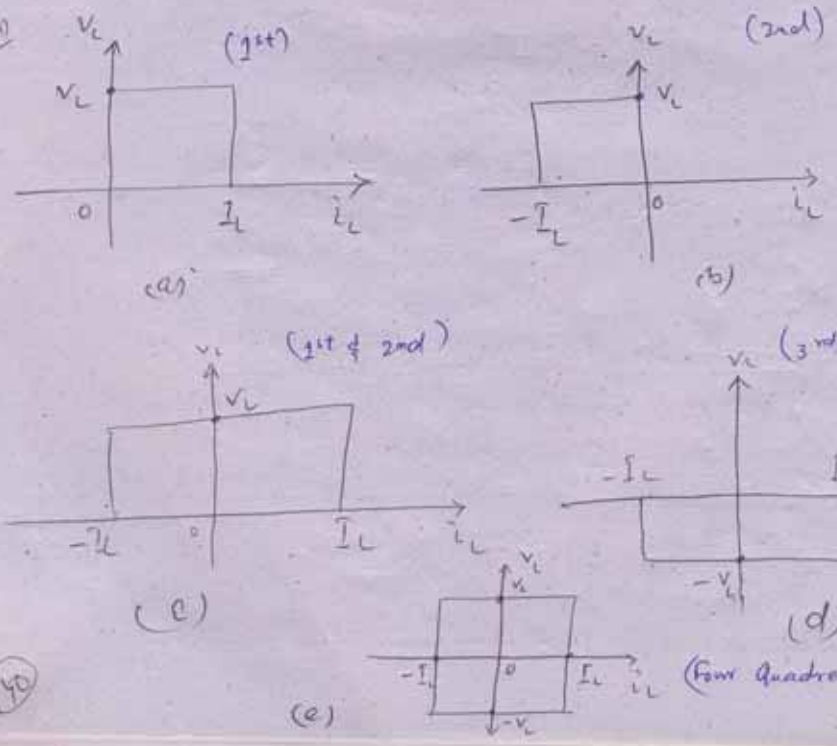
(3)

Converter Classification

09

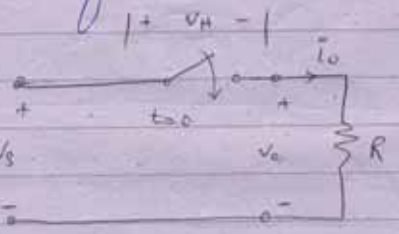
* Depending upon direction of current and voltage flow, dc converter can be classified to 5 type
  - First Quadrant converter
  - 2nd " "
  - 1st & 2nd Quad "
  - Third & 4th Quad "
  - Four quadrent "

(4)



1st Quad Converter:

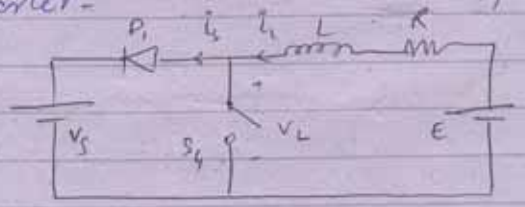
The load current flows into load. Both V & I are +ve. This is rectifier mode of operation of converter.



2nd Quad Converter:

(7)

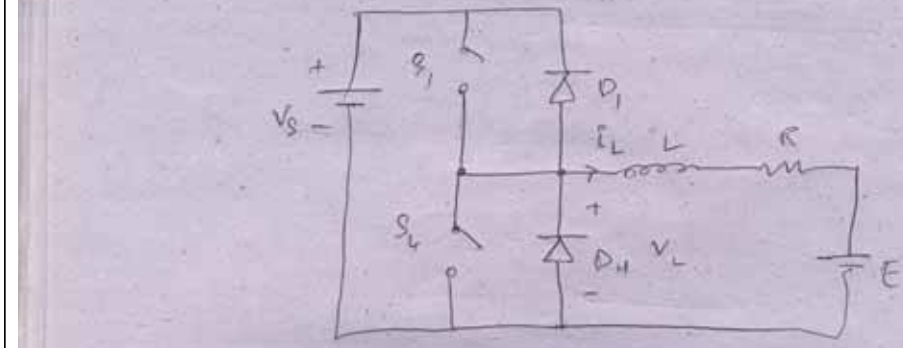
The i_L flows out of load. The load voltage is +ve but current is -ve. This is Inverter mode operation of converter.



1st and 2nd Quad:

(9)

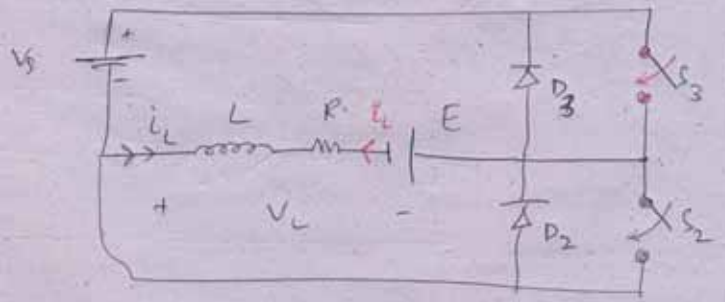
I_L is either +ve or -ve but V_L is always +ve. This type of converter can be either be operated as rectifier or an inverter.



3rd and 4th Quad:

(11)

I_L is either +ve or -ve but V_L is always -ve. Can be operated as rectifier or an inverter.



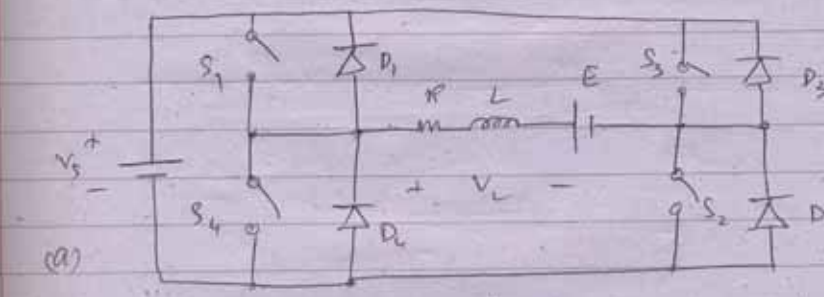
(* inverter mode) (* Rectifier mode)

(15)

08, 05, 08

(13)

Four Quad Converter : This form basis of single ϕ full bridge inverter- the V and I both can be +ve ~~and~~ or -ve and a full control over power flow is available.



(a)

(H- bridge Inverter)

(b)

Inv	Rect	S_4 (mod), D_2	S_1 (modulating)
$V_L + V_e$	$V_L + V_e$		S_2 (continue ON)
$i_L - V_e$	$i_L + V_e$	D_1, D_2	S_2, D_4
$V_L - V_e$	$V_L - V_e$	S_3 (mod)	S_2 (modulating), D_4
$i_L - V_e$	$i_L + V_e$	S_4 (cont. ON) S_4, D_2	D_3, D_4
Rect	inverter		

(b) (Polarity) (c) Conducting devices

(08, 05

Switching mode Regulators

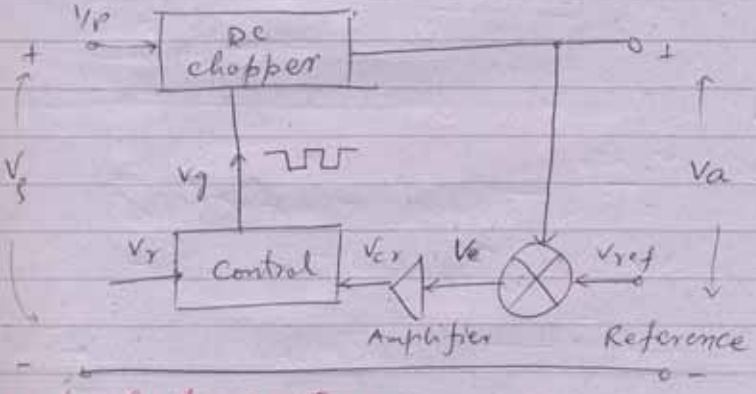
* Chopper : Pulse width controlling.
* DC conv can be used as switching mode regulator to convert un-regulated DC to regulated DC.
* PWM technique at constant freq is usually employed for that.
* Switching device may be BJT, MosFet or IGBT.
* Switching regs are commercially available in IC packages.

(19)

* The designer has to only choose external R & C value of oscillator reference.
* As a rule of thumb, to max 'η' the min oscillator period should be about 100 times long

than transistor switching time. If transistor has switching time of about 0.5 μsec, the oscillator must oscillate at min period of 50 μ sec, w/c gives max oscillator freq of about 20kHz.

A general switching mode regulator is shown below.



closed loop system.

+ve V_e (error voltage) → V_a

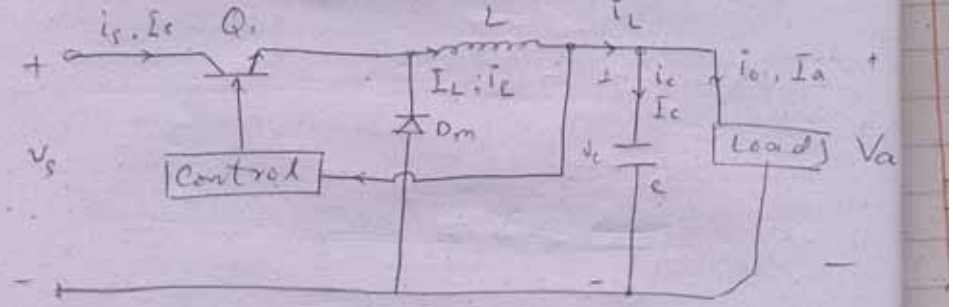
09,05,08

Switching mode regulator

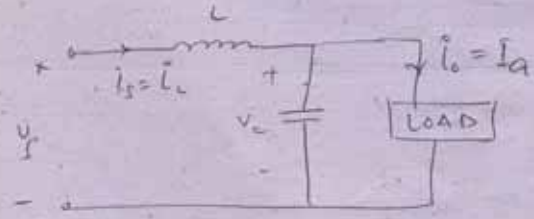
Classification

1. Buck regulator (2) Boost reg
3. Buck-boost (4) Cúk reg.

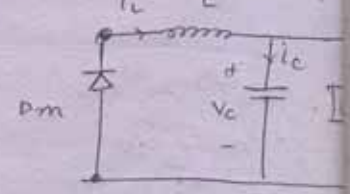
1- Buck Regulator:



* Modes:
  - Trans. conducting
  - Trans. not " "

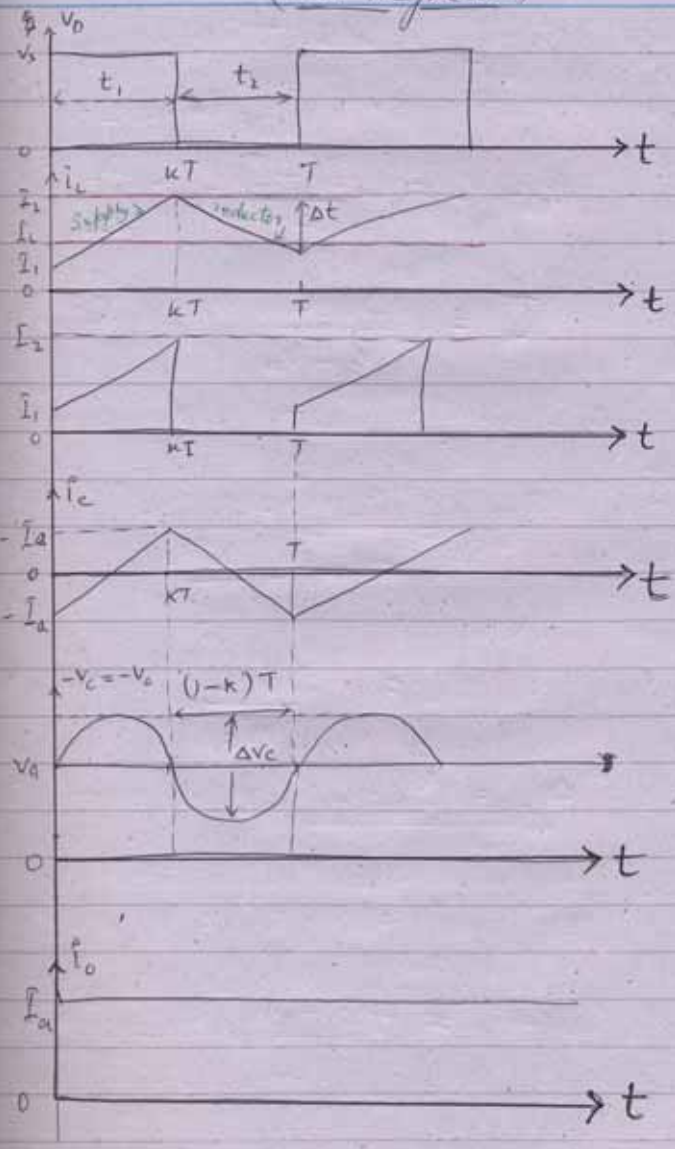


Mode (1)



Mode (2)

(Buck Regulator)



(25)

The voltage across 'L' is,

$$e_L = L \frac{di}{dt}$$

Assuming that inductor current rises linearly from I_1 to I_2 in time t_1

$$V_s - V_a = L \frac{I_2 - I_1}{t_1} = L \frac{\Delta I}{t_1} \quad (5.$$

$$t_1 = \frac{\Delta I L}{V_s - V_a} \quad (5.45)$$

and inductor current falls linearly from I_2 to I_1 in time t_2.

$$-V_a = -L \frac{\Delta I}{t_2} \quad (5.4$$

$$t_2 = \frac{\Delta I L}{V_a} \quad (5.47)$$

where $\Delta I = I_2 - I_1$ is peak to peak ripple current of inductor. Equating value of ΔI in Eqs. (5.44) & (5.46) we get

$$\Delta I = \frac{(V_s - V_a) t_1}{L} = \frac{V_a t_2}{L}$$

(22)

Substituting $t_1 = kT$ and $t_2 = (1-k)T$ yield average o/p voltage as

$$V_a = V_s \frac{t_1}{T} = k V_s \quad (5.48)$$

Assuming a lossless ckt

$$V_s I_s = V_a I_a = k V_s I_a$$

and i/p current (average)

$$I_s = k I_a \quad (5.49)$$

The switching period T can be expressed as

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I L}{V_s - V_a} + \frac{\Delta I L}{V_a}$$

$$T = \frac{\Delta I L V_s}{V_a (V_s - V_a)} \quad (5.50)$$

w/c gives p-p ripple current as

$$\Delta I = \frac{V_a (V_s - V_a)}{f L V_s} \quad (5.51)$$

or

$$\Delta I = \frac{k V_s (1-k)}{f L} \quad (5.52)$$

Using kirchoff's law of current we can write inductor current

$$i_L = i_c + i_o \quad (5.$$

If we assume that load ripple current Δi_o is very small and negligible $\Delta i_L = \Delta i_c$ (5.5

The avg cap current, w/c flows into for $\frac{t_1}{2} + \frac{t_2}{2} = \frac{T}{2}$ is

$$I_c = \frac{\Delta I}{4}$$

The cap voltage is expressed as

$$V_c = \frac{1}{C}\int i_c \, dt + V_c(t=0)$$

- peak-to-peak ripple ~~current~~ voltage of cap is

$$\Delta V_c = V_c - V_c(t=0) = \frac{1}{C}\int_0^{T/2} \frac{\Delta I}{4} dt = \frac{\Delta I T}{8C}$$

$$\Delta V_c = \frac{\Delta I}{8fC} \quad (5.$$

14-05-08

Substituting value of ΔI from eq (5.51) or (5.52) in eq (5.53) yields

$$\Delta V_c = \frac{V_a(V_s - V_a)}{8LCf^2 V_s} \quad (5.54)$$

$$\Delta V_c = \frac{V_s k(1-k)}{8LCf^2} \quad (5.55)$$

Condition for continuous L current and capacitor voltage:

If I_L is average inductor current, inductor ripple current $\Delta I = 2I_L$

using eqs (5.48) and (5.52), we get

Conduct : $\Delta I = I_L - (-I_L) = 2I_L$

$$\frac{V_s(1-k)k}{fL} = 2I_L = 2I_a = \frac{2kV_c}{R}$$

It gives critical value of inductor L_c as

$$L_c = L = \frac{(1-k)R}{2f} \quad (5.56)$$

If V_c is avg cap voltage, cap o/p voltage $\Delta V_c = 2V_a$. using (5.48) & (5.51) we get

$\Delta V_c = V_c - (-V_c) = 2V_c$

$$\frac{V_s(1-k)k}{8LCf^2} = 2V_a = 2kV_s$$

It gives critical value of Cap

$$C_2 = C = \frac{1-k}{16Lf^2} \quad (5.57)$$

(15-05-08)

* Single transistor based Buck regulator has η greater than 90% → (only single active element i.e PCT Tr)
* High di/dt is limited by L
* But i/p current is discontinuous and a i/p smoothing filter is generally required → limitation of Buck regulator
* Protection ckt is required in case of short ckt across diode.
* One polarity of o/p voltage with unidirection o/p current.

5.5 Finding values of LC filter for Buck regulator?

$V_s = 12\,V$, $V_a = 5\,V$ (average required) $R = 500\,\Omega$ and p-p o/p ripple voltage is 20 mV. The frequency is 25 kHz. If p-p ripple current is limited to 0.8 A, Determine:

(a) k (b) L (c) C and

(d) Critical value of L & C.

Sol: eq (5.52)

$$\Delta I = \frac{V_a (V_s - V_a)}{f L V_s}$$

(5.41)

$$k = \frac{V_a}{V_s} = \frac{5}{12} = 0.42$$

eq (5.52) gives

$$L = \frac{V_a (V_s - V_a)}{f \Delta I V_s}$$

$$L = \frac{5(12-5)}{(25k)(0.8)12}$$

$$L = 145.8\,\mu H$$

eq (5.55) $\Delta V_c = \frac{V_s k(1-k)}{8LCf^2}$ $\boxed{C = 200\,\mu F}$

$$C = \frac{V_s (k)(1-k)}{8 L \Delta V_c f^2} \Rightarrow C = \frac{12(0.42)(1-0.42)}{8(145.8\,H)(20m)(25k)^2}$$

(5.56)

$$L_c = \frac{(1-k)R}{2f}$$

$$= \frac{(1-0.42)500}{2(25k)}$$

$$L_c = 5.8\,m H$$

(5.57)

$$C = \frac{1-k}{16 L f^2}$$

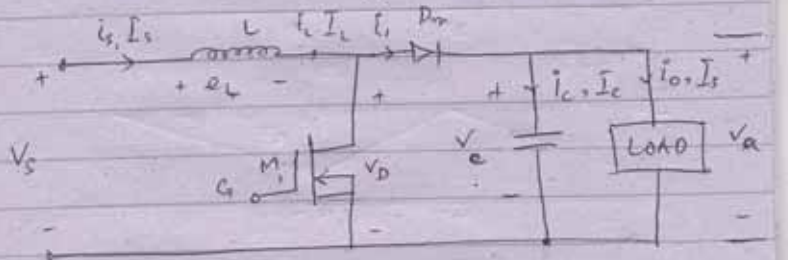
$$= \frac{1-0.42}{16 (5.8\,m)(25k)^2}$$

$$C = 10\,\eta F$$

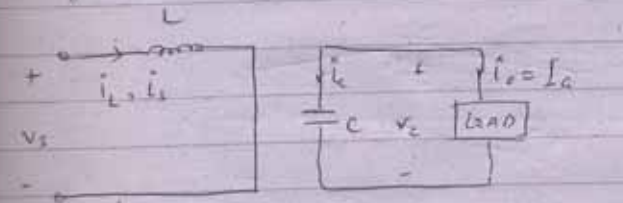
15-05-08

(Week: 15)

Boost Regulator

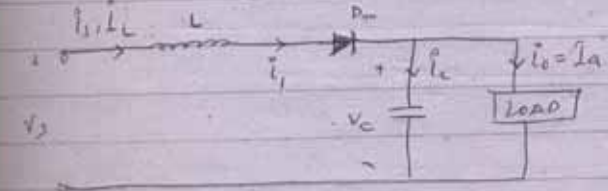


* Inductance is shifted in i/p.
* Switching element is in || with o/p.
* Diode is shifted after switch so only one gate goes on.

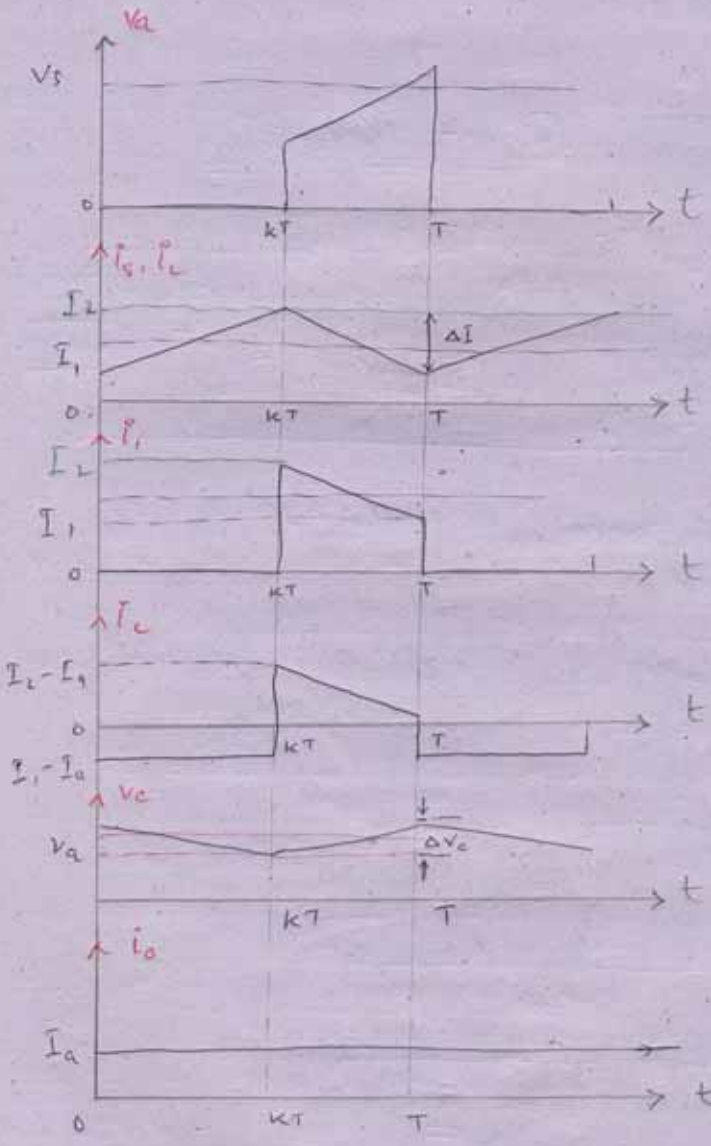


(Mode 1)

* Load is being supplied by capacitor



(Mode 2)



Assuming inductor current rises linearly from I_1 to I_2 in time t_2

$$V_s = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \quad (5.58)$$

or

$$t_1 = \frac{\Delta I L}{V_s} \quad (5.59)$$

and inductor current falls from I_2 to I_1 in time t_2

$$V_s - V_a = -L\frac{\Delta I}{t_2} \quad (5.60)$$

or

$$t_2 = \frac{\Delta I L}{V_a - V_s} \quad (5.61)$$

where $\Delta I = I_2 - I_1$ = peak-peak ripple current of 'L' from eq. (5.58) and (5.60)

$$\Delta I = \frac{V_s t_1}{L} = \frac{(V_a - V_s)t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1-k)T$ yields average o/p voltage

$$V_a = V_s\frac{T}{t_2} = \frac{V_s}{1-k} \quad (5.62)$$

which gives

$$(1-k) = \frac{V_s}{V_a} \quad (5.63)$$

substituting $k = \frac{t_1}{T} = t_1 f$ in 5.63)

$$t_1 = \frac{V_a - V_s}{V_a f} \quad (5.64)$$

Assuming a lossless ckt $V_s I_s = V_a I_a$

$V_s I_a/(1-k)$ and avg i/p current

$$I_s = \frac{I_a}{1-k} \quad (5.65)$$

Thus switching period T can be found

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I L}{V_s} + \frac{\Delta I L}{V_a - V_s}$$

$$T = \frac{\Delta I L V_a}{V_s(V_a - V_s)} \quad (5.$$

(91)

and this gives p-p ripple current

$$\Delta I = \frac{V_s(V_a - V_s)}{f V_a L} \quad (5.67)$$

or

$$\Delta I = \frac{V_s k}{fL} \quad (5.68)$$

when transistor is on, cap supplies load for $t = t_1$. The avg cap current during time t_1 is $I_c = I_a$ and p-p ripple voltage of cap is

$$\Delta V_c = V_c - V_c(t=0) = \frac{1}{C}\int_0^{t_1} I_c\,dt = \frac{1}{C}\int I_a$$

$$\Delta V_c = \frac{I_a t_1}{C} \quad (5.69)$$

Substituting $t_1 = \frac{(V_a - V_s)}{V_a f}$ from (5.64)

$$\Delta V_c = \frac{I_a(V_a - V_s)}{V_a f C} \quad (5.70)$$

or

$$\Delta V_c = \frac{I_a k}{fC} \quad (5.71)$$

Condition for continuous current Inductor and Capacitor voltage:

If I_L is avg L current, inductor ripple current $\Delta I_L = 2I_L$.

Eq (5.62) and (5.68) we get

$$\frac{kV_s}{fL} = 2I_L = 2I_a = \frac{2V_s}{(1-k)R}$$

which gives critical value of L as

$$L_c = L = \frac{k(1-k)R}{2f} \quad (5.7$$

If V_c is avg Cap voltage capacitor ripple voltage $\Delta V_c = 2V_c$ eq (5.71) we get

$$\frac{I_a k}{Cf} = 2V_a = 2I_a R$$

which give critical value of Cap

$$C_c = C = \frac{k}{2fR} \quad (5.73)$$

(160)

(Boost Regulator)

Circuit properties: (11)

Boost reg step up voltage without a trfr & high η due to single transistor operation.

I/p current is contenous, however a high peak current has to flow thru the tranr. → (High PIV rating req)

O/p voltage is very sensitive to duty cycle (k).

Stabilization of o/p voltage can be a problem.

Solution: Use ripple filter at o/p.

The avg o/p current is < average inductor current by a factor 1−k.

Much higher rms current to flow thru filter cap.

Hence larger filter cap and inductor than buck reg are required.

(12)

Ex: 5.6 $V_s = 5V$, $V_a = 15V$, $I_a = 0.5A$.
$f = 25kHz$. $L = 150\mu H$ and $C = 220\mu$
determine (a) k (b) ΔI (c) I_2
(d) ΔV_c. (e) Critical L_c & C_c.

Sol^n

eq (5.63)

$$k = 1 - \frac{V_s}{V_a}$$

(a) $$k = 0.667$$

eq (5.60)

(b) $$\Delta I = \frac{V_s k}{fL}$$

$$= \frac{(5)(0.667)}{(25k)(150\mu)}$$

$$\Delta I = 0.89\ A$$

eq (5.

(c) $$I_2 = I_s + \frac{\Delta I}{2}$$

$$= 15 + \frac{0.89}{2}$$

$$I_2 = 1.945$$

eq (5.

(d) $$\Delta V_c = \frac{I_a k}{fC}$$

$$= \frac{(0.5)(0.667)}{(25k)(220\mu F)}$$

(162) $$\Delta V_c = 60.63\ mV$$

15,05,08

(e) $L_c = \frac{k(1-k)R}{2f}$

$R = \frac{V_a}{I_a} = \frac{15}{0.5} = 30\Omega$

$L_c = \frac{(0.667)(1-0.667)30}{2(25k)}$

$L_c = 133\,\mu H$

$C_c = \frac{k}{2fR}$

$= \frac{0.667}{2(25k)30}$

$C_c = 444.6\,\eta F$

15

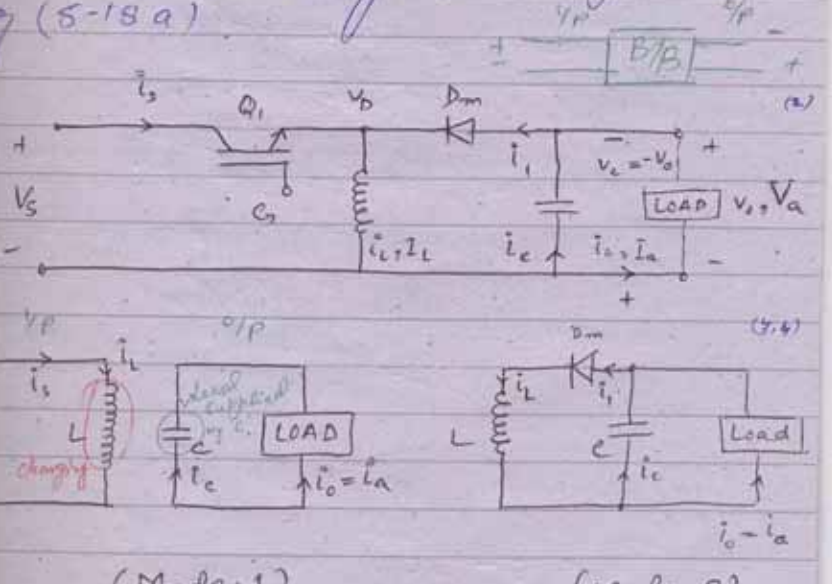
Q/⇒ Rework the problem by taking duty cycle = 60%

Q/⇒ Rework problem when switching freq is altered to 50kHz with k ⇒ (1) 66% (2) 60%.

21-05-07

BUCK-BOOST

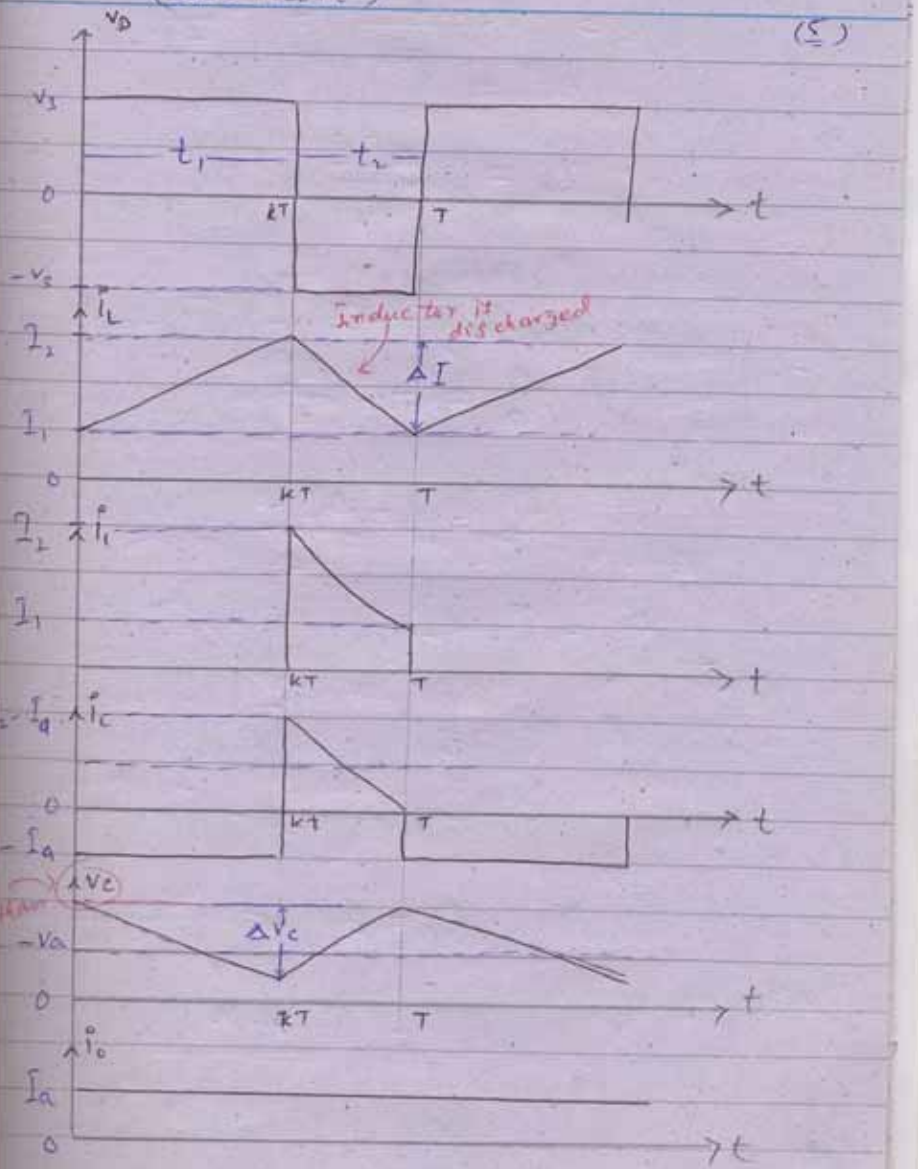
A buck-boost reg provides an o/p voltage that may be less than or greater than i/p voltage - hence name "Buck-Boost". o/p voltage polarity is opposite to that of i/p voltage. This reg is also known as "an inverting regulator". The ckt arrangement of a buck-boost reg is shown in fig (5-18a)



The ckt operation can be divided into two modes. During mode 1, transistor is turned ON and diode D_m is reverse biased. The i/p current, which rises, flows thru 'L' and Q_1. During mode 2 trans Q_1 is switched off and current, which was flowing thru L would flow thru L, C, D_m and load. The energy stored in inductor would be transferred to load and the inductor current fall until trans Q_1 is switched ON again in next cycle. The equivalent ckts for modes are shown. The waveforms for steady state voltage and current of B-B reg are shown in (fig 5-18c) for continuous load current.

21-05-08

(Back Board)



Assuming that inductor current rises linearly from I_1 to I_2 in time t_1

$$V_s = L \frac{I_2 - I_1}{t_1} = L \frac{\Delta I}{t_1} \qquad (5.7$$

or

$$t_1 = \frac{\Delta I L}{V_s} \qquad (5.75)$$

i_L falls linearly from I_2 to I_1 in t_2

$$V_a = -L \frac{\Delta I}{t_2} \qquad (5.76)$$

$$t_2 = -\frac{\Delta I L}{V_a} \qquad (5.77)$$

where $\Delta I = I_2 - I_1$ = p-p ripple current of inductor 'L' from eqs (5.74) and (5.76)

$$\Delta I = \frac{V_s t_1}{L} = -\frac{V_a t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1-k)$ avg o/p

$$V_a = \frac{V_s k}{1-k} \qquad (5.7$$

(168)

21-09-09

(Buck-Boost)

Substituting $t_1 = kT$ and $t_2 = (1-k)T$ into eq 5.79

$t_1 = kT$ and $t_2 = (1-k)T$ into

(5.78)

$$(1-k) = \frac{-V_s}{V_a - V_s} \qquad (5.79)$$

Substituting $t_2 = (1-k)T$ and $(1-k)$ from eq (5.79) in eq (5.78) yields

$$t_1 = \frac{V_a}{(V_a - V_s)f} \qquad (5.80)$$

Assuming lossless ckt

$V_s I_s = -V_a I_a = \frac{V_s I_a k}{1-k}$ and avg i/p current is related to avg o/p current I_a by

$$I_s = \frac{I_a k}{1-k} \qquad (5.81)$$

The switching period T can be found from

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I_L}{V_s} + \frac{\Delta I_L}{V_a} \qquad (5.82)$$

$$T = \frac{\Delta I_L (V_a - V_s)}{V_s V_a}$$

and gives p-p ripple current

$$\Delta I = \frac{V_s k}{f L} \qquad (5$$

or

$$\Delta I =$$

* when Q_1 is ON, filter cap supplies load current for $t = t_1$. The avg discharging current of cap, $I_c = I_a$ and peak-pk ripple vol of cap is

$$\Delta V_c = \frac{1}{C}\int_0^{t_1} I_c\,dt = \frac{1}{C}\int_0^{t_1} I_a\,dt$$

$$\Delta V_c = \frac{I_a t_1}{C} \qquad (5.85)$$

Substituting $t_1 = \frac{V_a}{(V_a - V_s)f}$ from eq(5. becomes;

$$\Delta V_c = \frac{I_a V_a}{(V_a - V_s) f C} \qquad (5$$

or

$$\Delta V_c = \frac{I_a k}{f C} \qquad (5$$

20-05-08

Condition for Continous inductor current &
" Capacitor voltage :

If I_L is avg inductor current, inductor ripple $\Delta I_L = 2I_L$ using eq (5.78) & (5.84) we get

$$\frac{kV_s}{fL} = 2I_L = 2I_a = \frac{2kV_c}{(1-k)R}$$

We gets critical value of L_c as

$$L_c = L = \frac{(1-k)R}{2f} \qquad (5.88)$$

If V_c is avg cap voltage, capacitor ripple voltage $\Delta V_c = 2V_a$ Using eq (5.87) we get

$$\frac{I_a k}{Cf} = 2V_a = 2I_a R$$

We give critical value of C

$$C_c = C = \frac{k}{2fR} \qquad (5.89)$$

(15)

* A B-B reg provides o/p voltage polarity reversal without trf/r
* It has high η.
* Under fault condition of tran di/dt is limited by inductor
* o/p short ckt protection is easy to implement.
* I/p current is discontinous & a high peak current flows thro tran Q1.

Ex 5.7 $V_s = 12V$, $k = 0.25$, $f = 25kHz$
$L = 1750\mu H$, $C = 220\mu F$. $I_a = 1.25A$.
Determine (a) V_a (b) ΔV_c (c) ΔI I_p (e) Critical L and C ?

Sol $\Delta V_c = \frac{I_a t_1}{C}$ 5.85

$t_1 = \frac{V_a}{V_s}$ $V_a = \frac{V_s k}{1-k}$ (5.

(17) $t_1 = \frac{V_a}{(V_s - V_s)f}$

(a) $V_a = \dfrac{V_s K}{(1-K) f}$

$= \dfrac{(12)(0.25)}{(1-0.25)\ 25K}$

$V_a = -4$

(b) $\Delta V_c = \dfrac{I_a t_1}{C}$ eq (5.37)

$t_1 = \dfrac{V_a}{(V_a - V_s) f}$

$\Delta V_c = \dfrac{I_a K}{f C}$

$= \dfrac{4}{(4-12)\ 25K}$

$\Delta V_c = 56.8\ mV$

$t_1 = 20\ \mu Sec$

$\Delta V_c = \dfrac{(1.25)(20\mu)}{220\mu}$

$\Delta V_c = -0.125\ V$

(c) $\Delta I = \dfrac{V_s \cdot K}{f L}$

$= \dfrac{(12)(0.25}{(25K)(150\mu)}$

$\Delta I = 0.8\ A$

(e) $L_c = \dfrac{(1-K) R}{2f}$ $\quad R = \dfrac{V_a}{I_a} =$

$L_c = \dfrac{(1-0.25)3.2)}{2(25K)}$

$L_c = 48\ \mu H$

$C = \dfrac{K}{2fR}$

$= \dfrac{0.25}{2(25K)\ 3.2}$

$C = 1.56\ \mu F$

(d) $I_s = \dfrac{1.25 \times 0.25}{(1-0.25)} = 0.4167A$

$I_p = \dfrac{I_s}{K} + \dfrac{\Delta I}{2}$

$= \dfrac{0.4167}{0.25} + \dfrac{0.8}{2}$

$I_p = 2.067\ A$

22-05-08

MOTOR DRIVES

(Introduction to Solid State Drives)

* In industrial application electrical motors are extensively used. (2')
* Both DC and AC motor are utilized in industry.
* Motor drives are ~~electrical~~ electronic ckts that can control speed & subsequently torque of these motors.
* Two types of drives:

  (i) DC Drives (ii) AC Drives

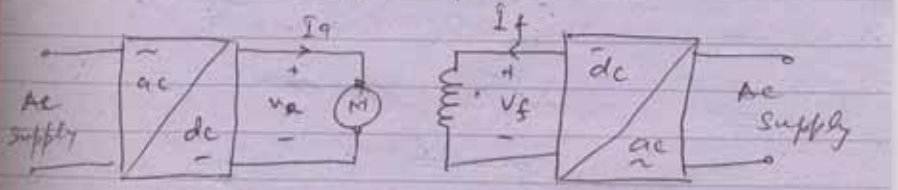
* DC motors have variable characteristics and are extensively used in industry.
* They can provide high starting torque and their speed can be controlled over a wide range.
* The methods of speed control are usually simpler and less expensive than ac motors.

* Both series and sperately excited m (dc) are used in variable speed dri
* Usually series motors are preferred for traction application.
* Due to commutators, dc motors are not recommended for high speed applications
* DC motors require more maintan as compared to ac motors.
* Modern advancements in power electronics have enabled ac moto drives to became more compet with dc drives. 2½
* Future belongs to ac drives but currently dc drives are mostly employed.
* It might be a few decades more when dc drives will fully b replaced by AC drives.
* Controlled rectifiers can general a variable dc o/p from ac I/p

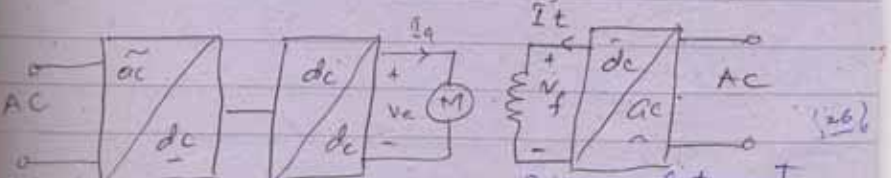
* A dc to dc converter can generate a variable dc o/p from a fixed dc i/p.

* The controlled rectifier and dc to dc converters have revolutionized dc drives concept and now variable speed dc drives have power levels from fractional horsepower to several mega watts.

* Controlled rectifier are generally used for speed control of dc motor as shown below:



{a) Controlled rect-fed drives}



{(b) Chopper fed drive}

* Speed of a dc motor can be varied by controlling (1) Armature voltage (2) Field current (3) Armature current that is a measure of torque demand.

* For a speed less than rated sp (also known as base speed) the arm voltage is varied to control spee while arm and field currents maintained constant. For a speed higher than rated speed, field current is varied to control speed while arm voltage is maintained at rated value.

* DC drives can be classified into 3 types:
  - Single ϕ
  - 3 ϕ
  - DC - DC converter drives.

(178)

22-05-08

AC motors are light weight (20 to 40% lesser than dc motor)
Expensive
low maintainance.
For variable speed they require freq and voltage & current.
Power converter, inverter & ac controllers can control freq, voltage & current to meet drive requirements. (29)

Two type of AC drives:
- Induction motor Drives
- Synchronous " "

Methods:
- stator voltage control.
- Rotar " "
- Frequency control. (30)