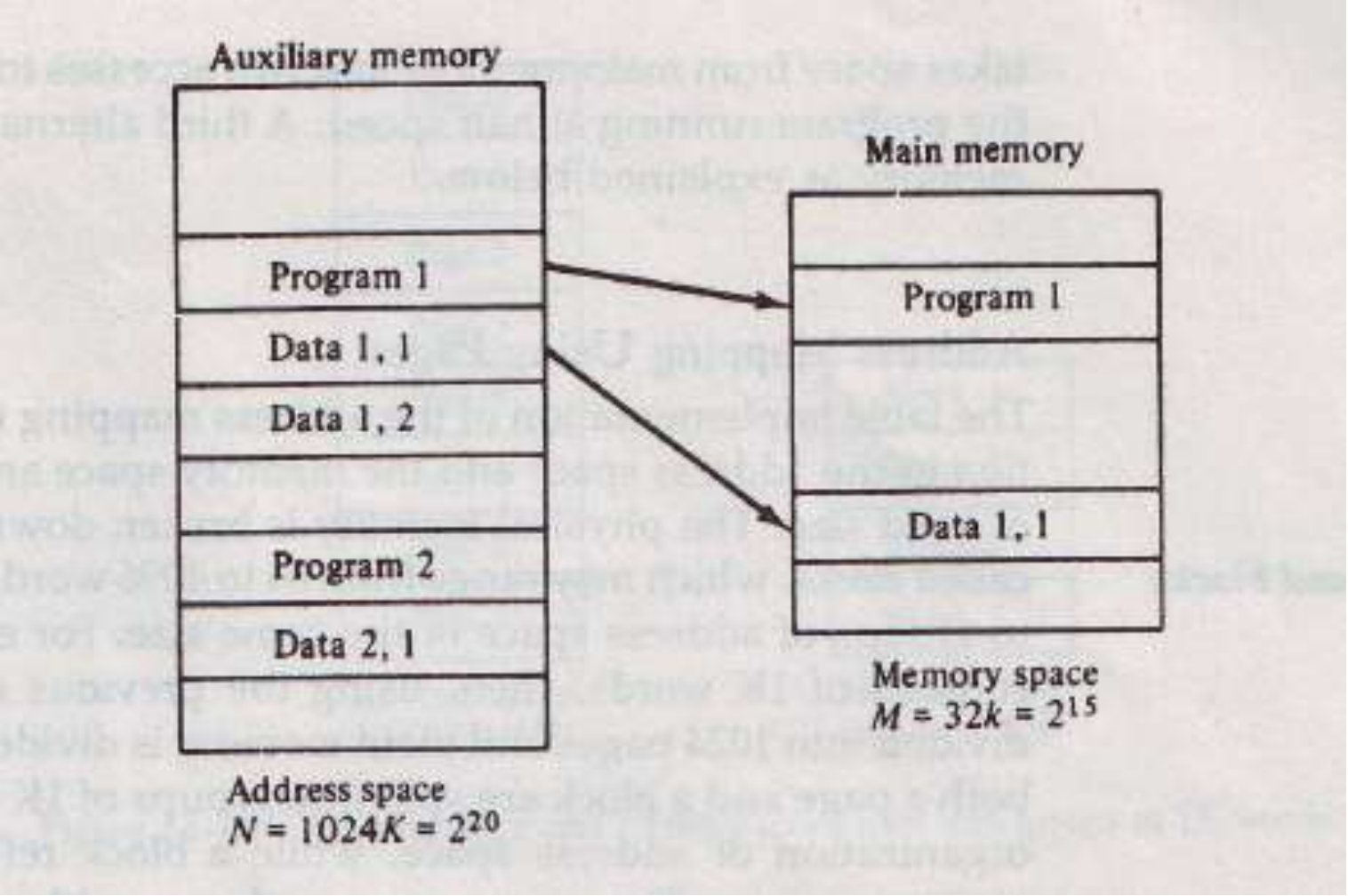
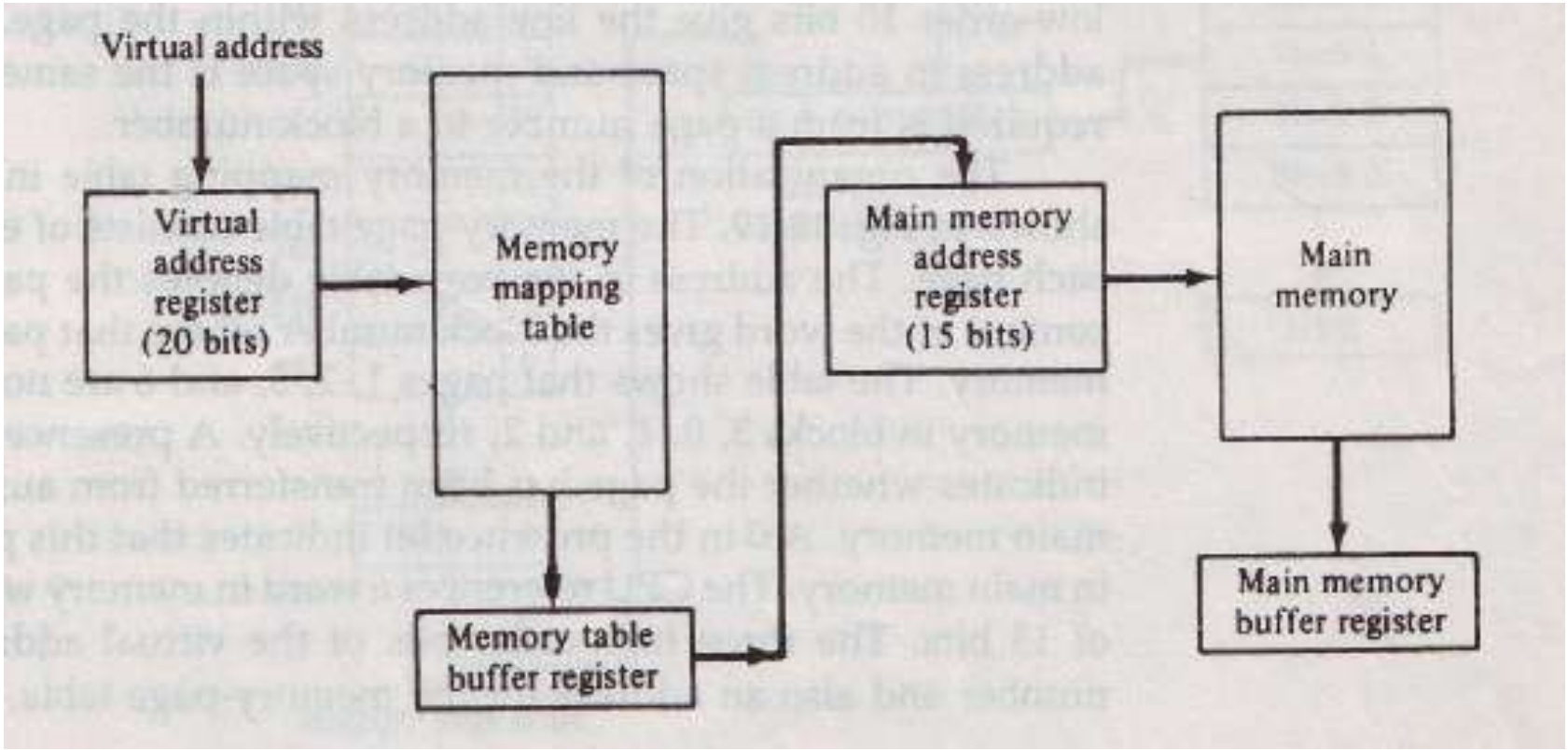
UNIT-4

Memory Organization

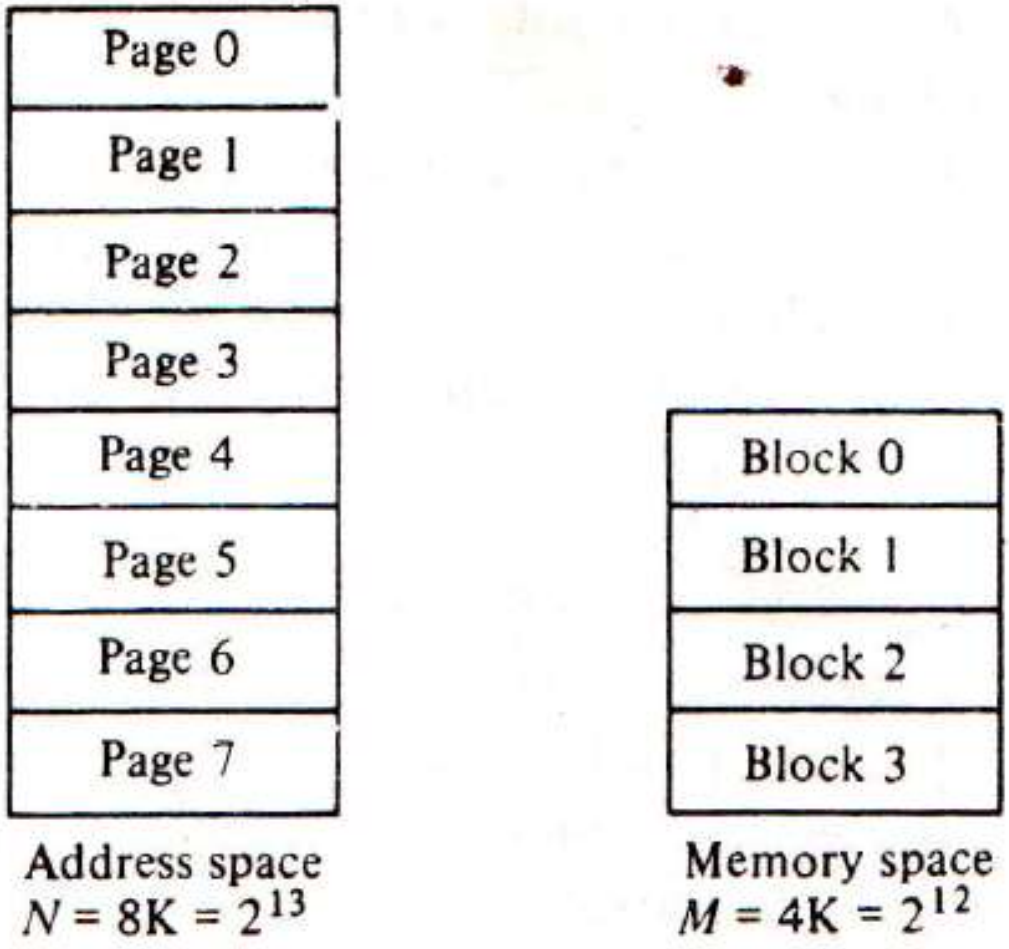
Address Space & Memory Space



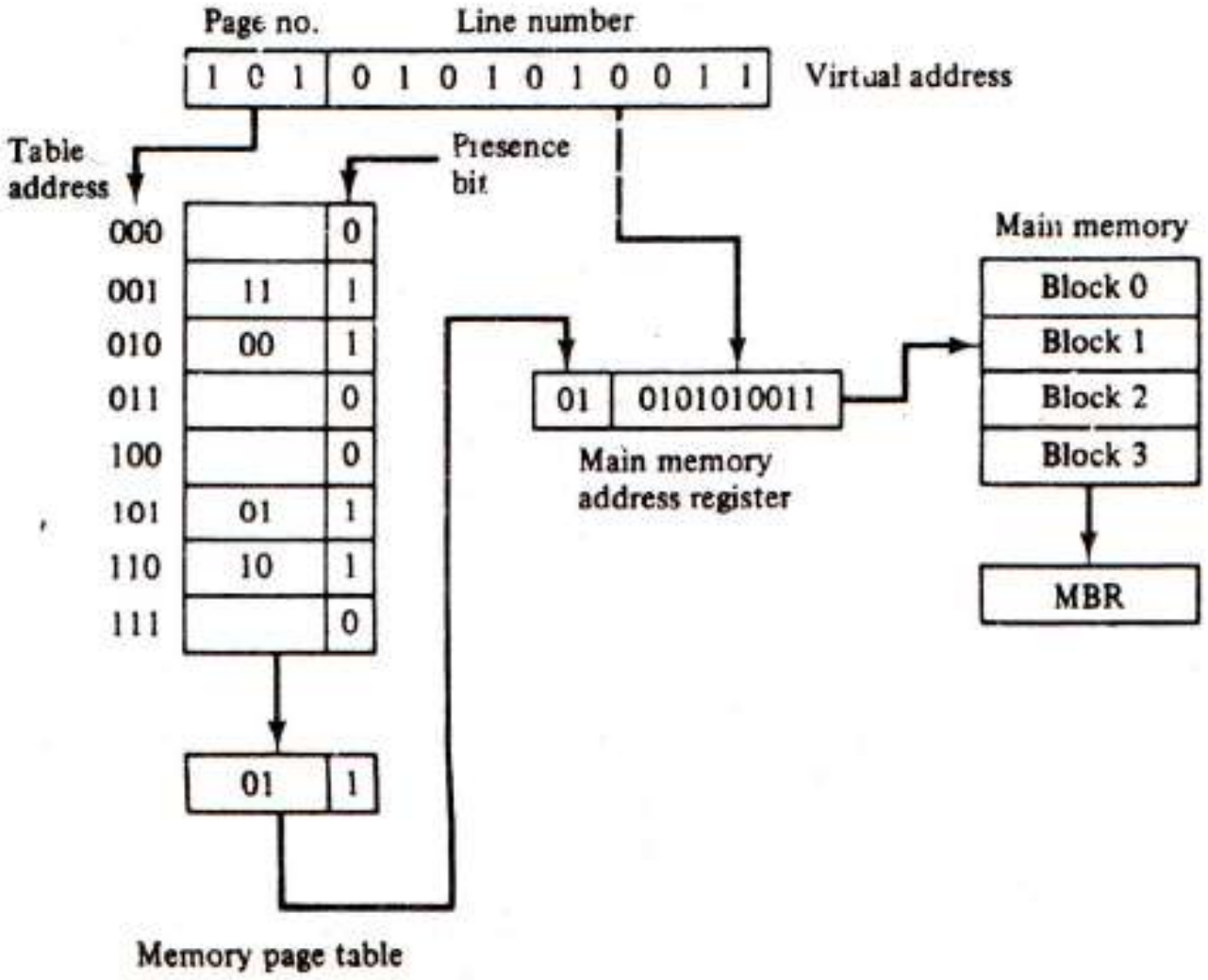
Memory Table For Mapping A Virtual Address:



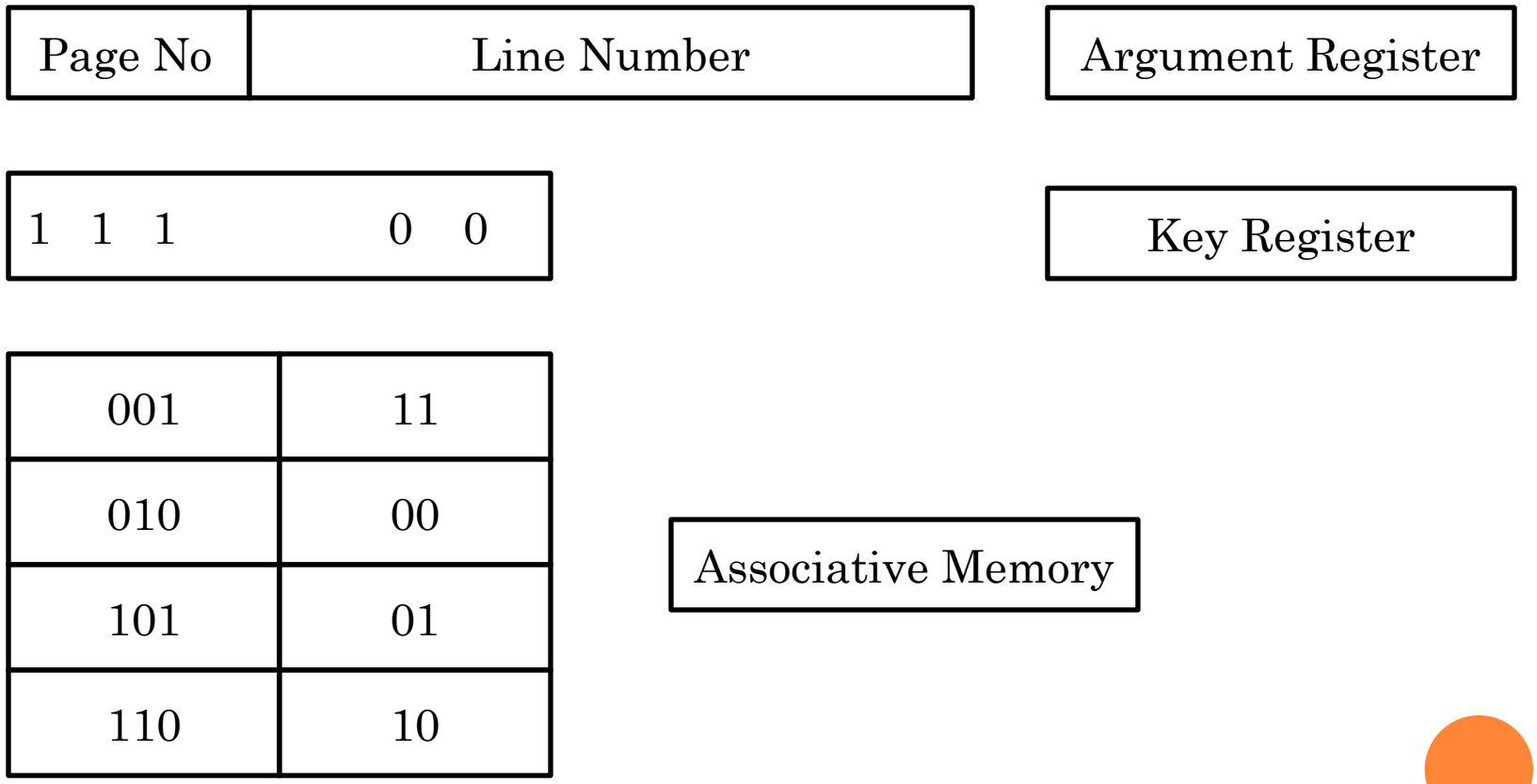
Address Space & Memory Space Split Into Groups:



Memory Table In A Paged System



An Associative Memory Page Table



Page Replacement Algorithm

- FIFO
- LRU
- OPT

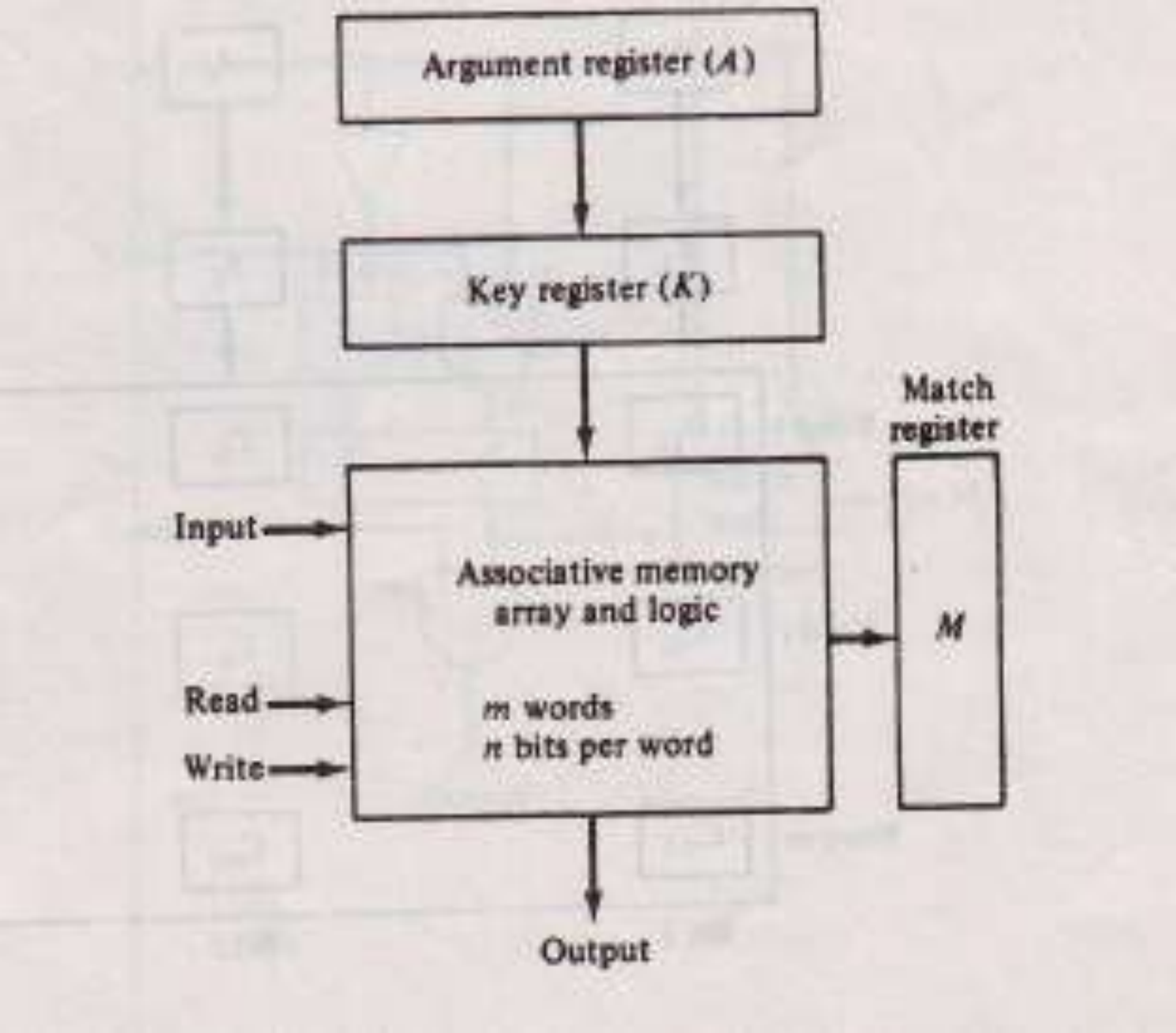
- Page No:

  2 3 2 1 5 2 4 5

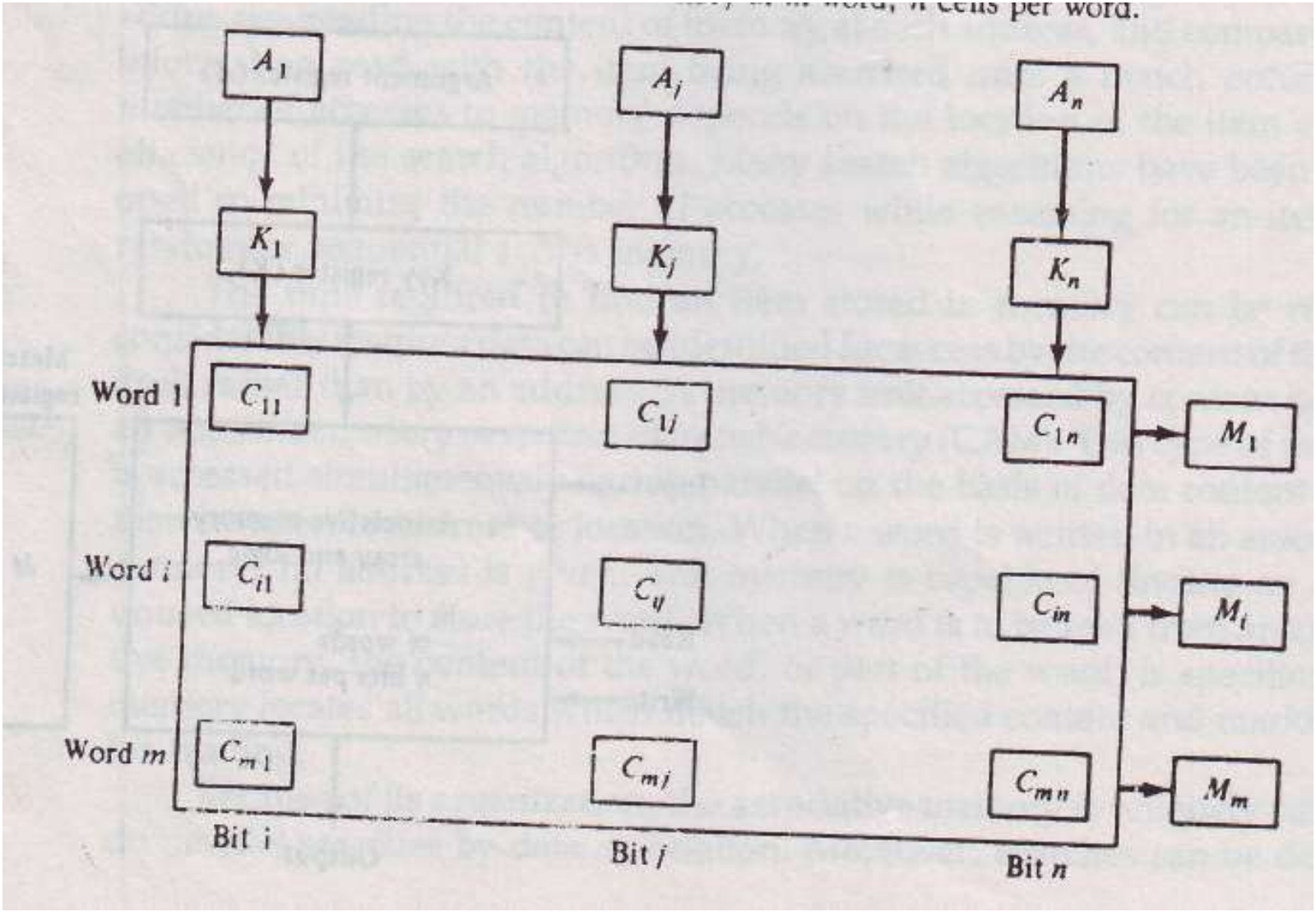
  3 2 5 2

- Total No of Frames:-3

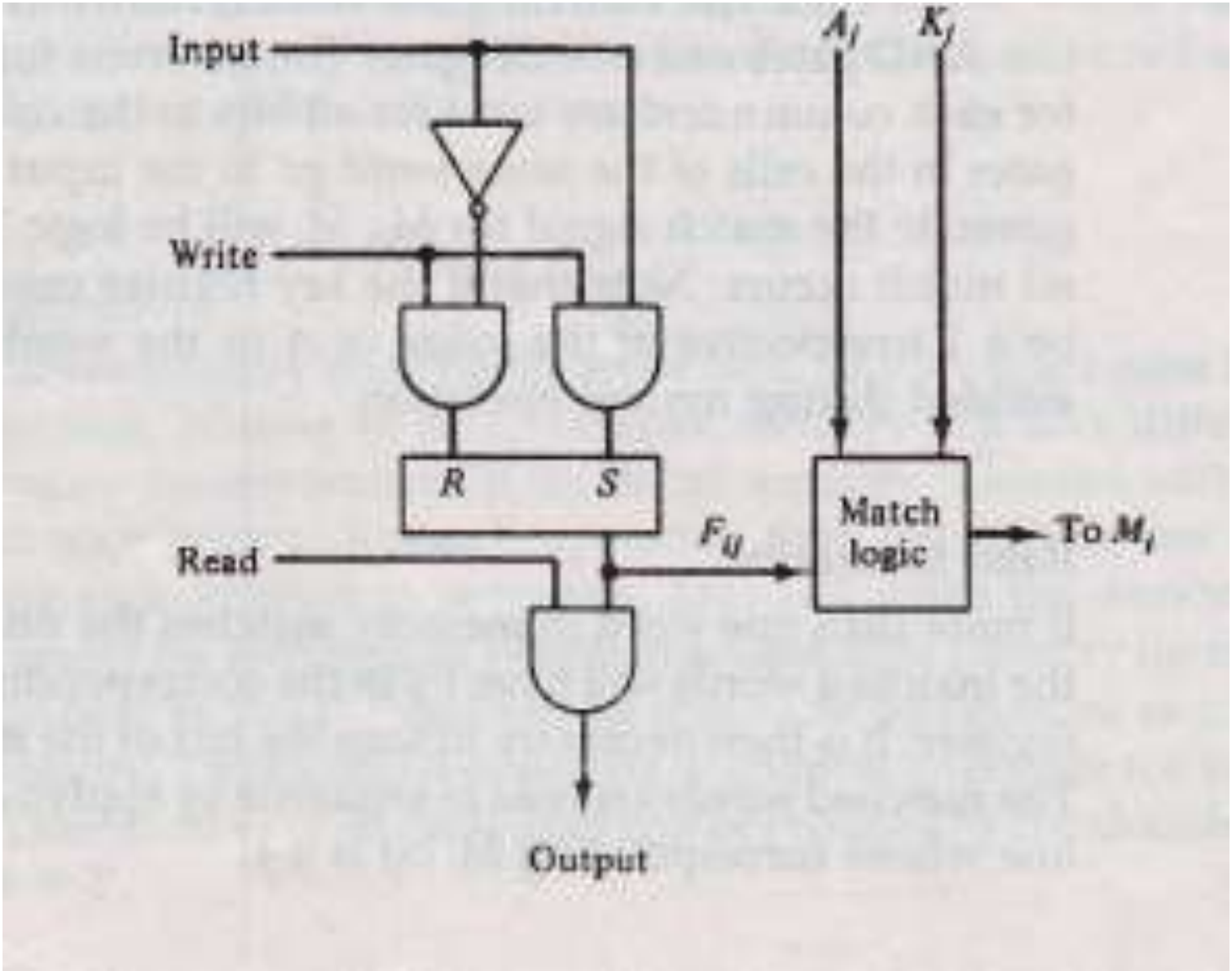
Associative Memory



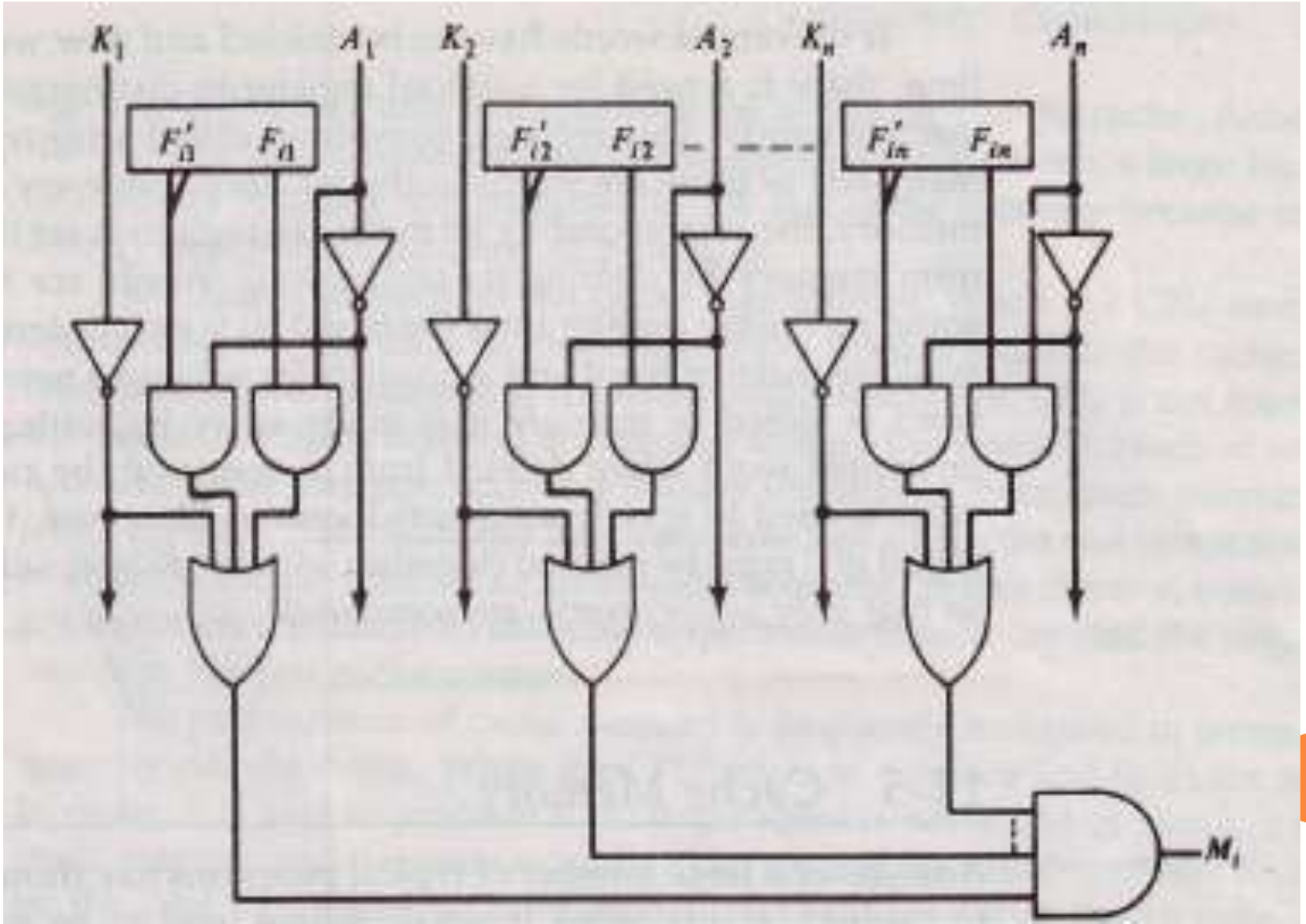
Associative Memory With M Words and N Bits/Word:



Each Cell Consist Of



Match Logic:



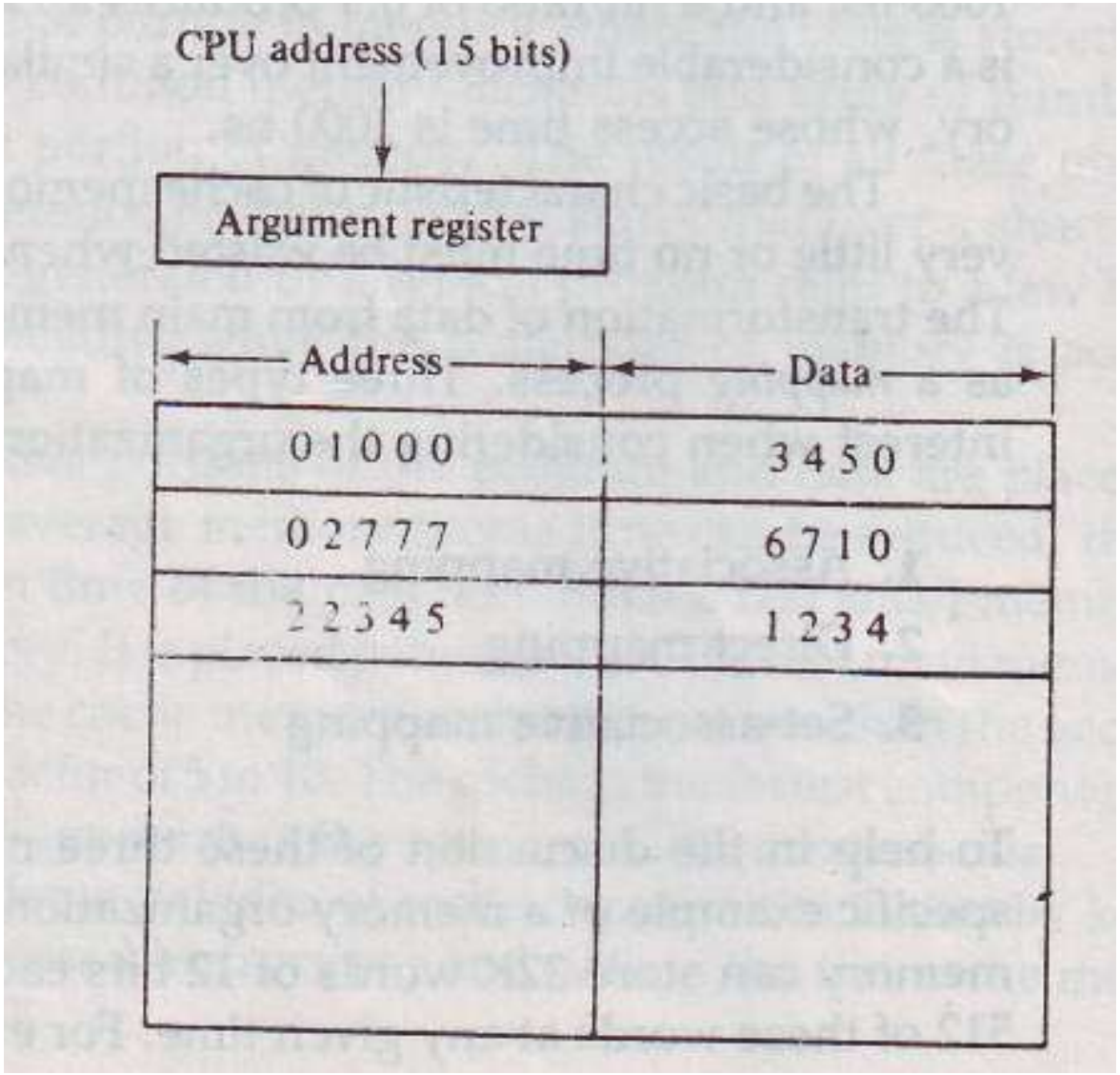
Cache Memory

- The active portions of the program and data are placed in a fast small memory then the average memory access time is reduced, such a fast small memory is known as cache memory.

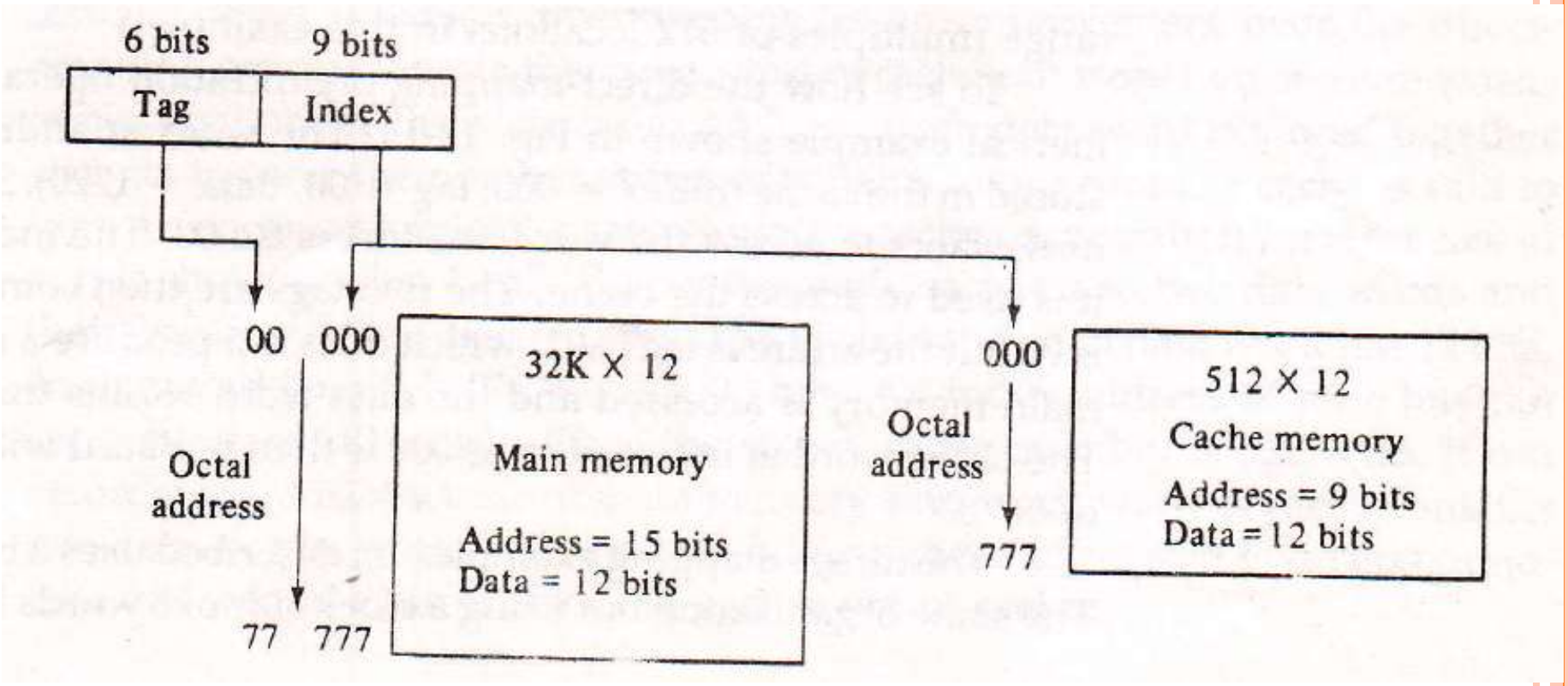
- When the CPU refers to the memory and finds the word in cache it means there is a hit and if it is not found in cache then it is a miss. The hit ratio can be calculated as:
  - No of Hits/Total No of References(hits+miss)

- There are 3 different types of mapping
  - Associative Mapping
  - Direct Mapping
  - Set Associative Mapping

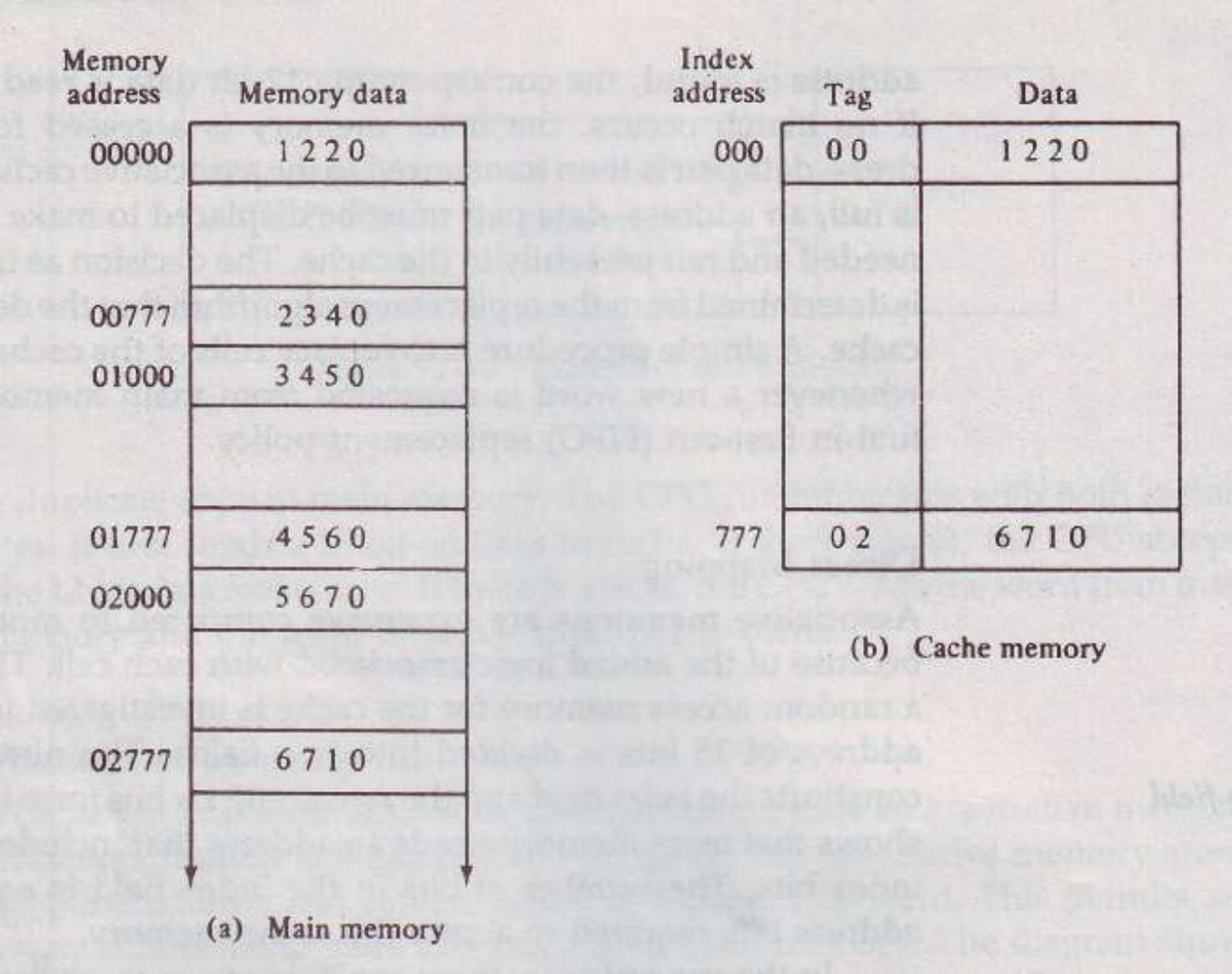
Associative Mapping



Direct Mapping (1)



Direct Mapping (2)



Direct Mapping By Using Blocks

If the direct mapping uses a block size of more than 1k words then each block consist of more than an individual data with different index number but with the same tag

Direct Mapping By Using Blocks (Contd…)

Block 0	000 007	01 01	3450 6578
Block1			
Block63	770 777	02 02	8891 6710

Set Associative Mapping

Index	Tag	Data	Tag	Data
000	01	3450	02	5670
777	02	6710	00	2340

Writing Into cache

- Write Through
- Write Back

- Valid Bit-→ Initially it is 0