UNIT-5

SYSTEM ORGANIZATION

Communication Methods

- There are 2 types of communication
  - Intersystem Communication
  - Intrasystem Communication

Communication Methods Contd…

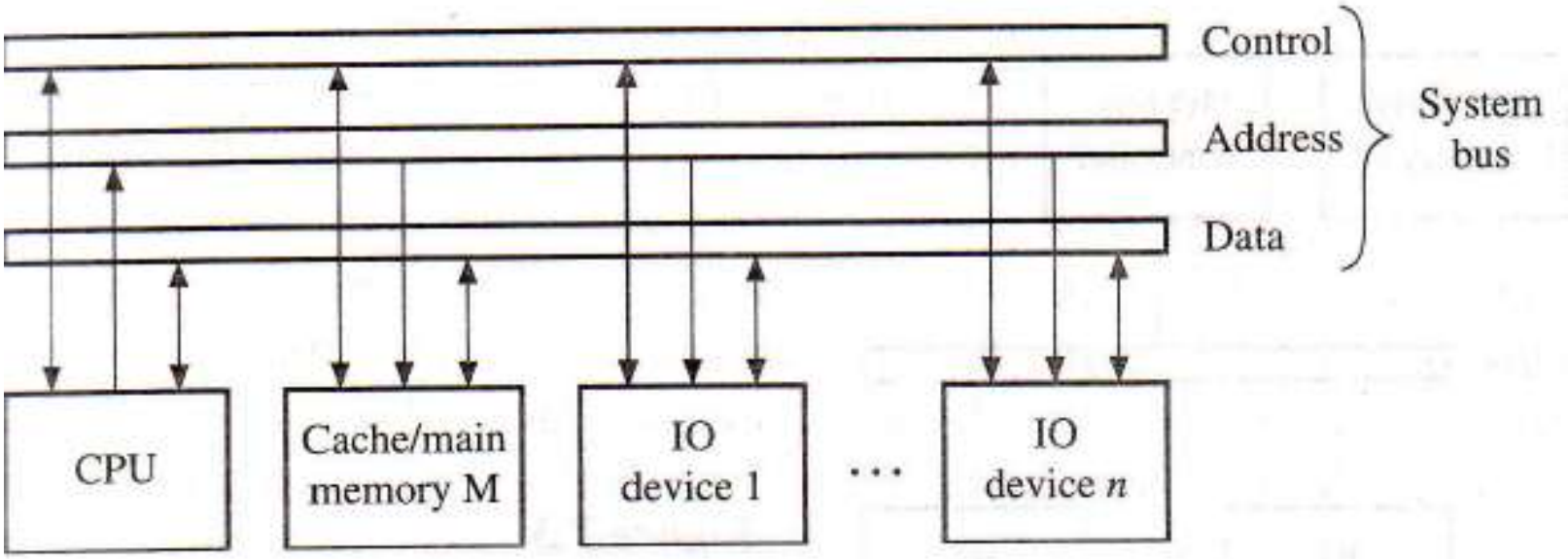
- Intrasystem communication occurs within a single computer system and involve system transfer over distances of less than a meter. It is primarily implemented by groups of electrical wires called buses.

- Intersystem communication means communication between the system by using a variety of physical media including electrical cables, optical fibers and wireless links. Here serial data transfer is preferred for communication because of longer distances.

BUS

- A Single Bus handles all intra system communication. All unit share the system bus, therefore at any given time only two units can communicate with each other.
- The CPU act as an active device or bus master & memory unit and I/O devices may act as a passive or slave unit.
- A bus typically consist of 3 group of lines i.e.
  - Address Lines 8 to 32
  - Data Lines 16 to 128
  - Control Lines

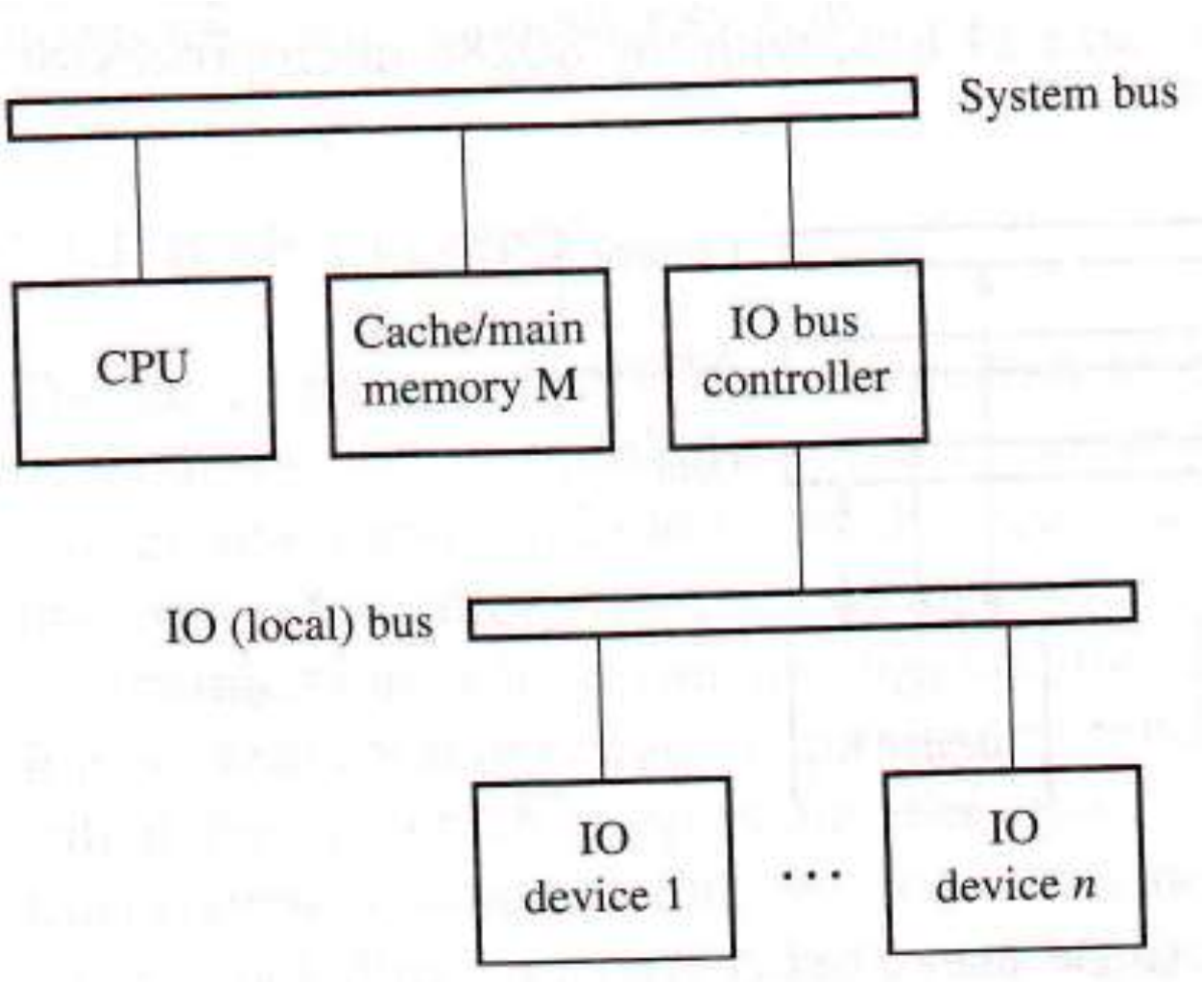
BUS Contd…


Control
Address
Data
System bus
CPU
Cache/main memory M
IO device 1
...
IO device n

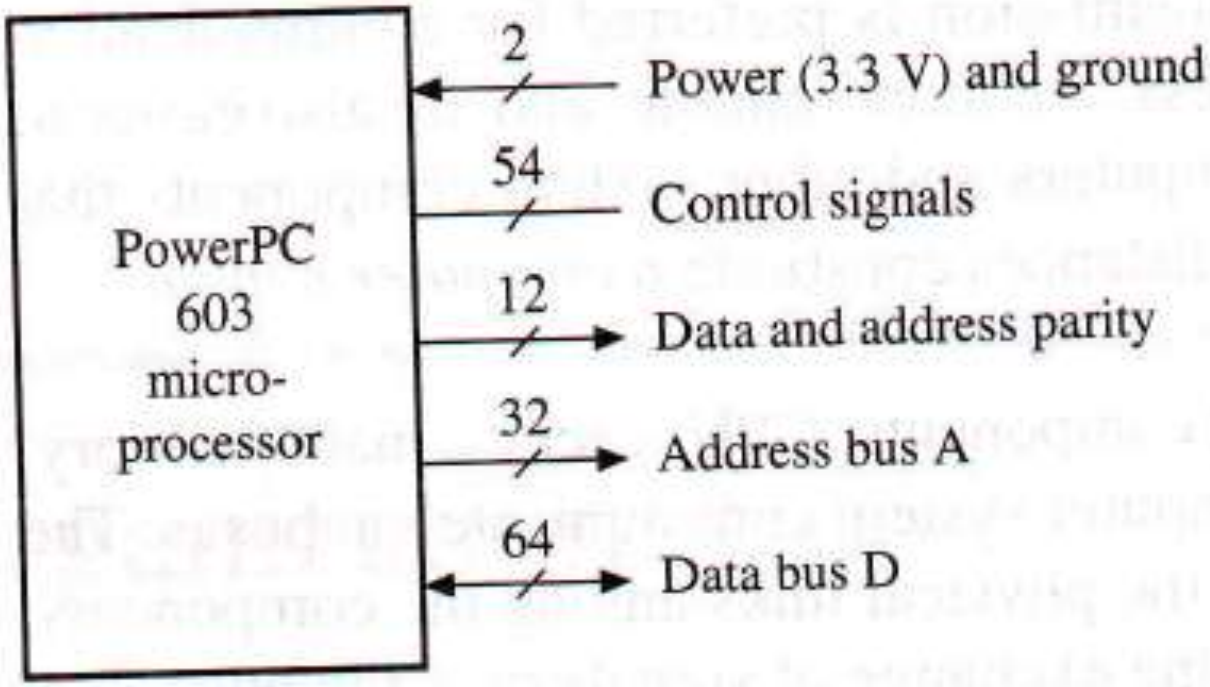
BUS Contd…

- The principal use of system bus is high speed data transfer between the CPU and main memory.
- Most I/O devices are slower than the CPU or M, therefore they need to be connected to the system bus by making use of an interface circuits called I/O Controller.
- A Single I/O controller can interface many I/O devices to the system bus. And this I/O controller is connected to many I/O devices by making use of I/O bus.

BUS Contd….


System bus
CPU
Cache/main memory M
IO bus controller
IO (local) bus
IO device 1
...
IO device n

For Eg: Power PC



Long Distance Communication

- Long Distance Communication can be done by making use of modem.

- A modem act as a
  - Modulator
  - Demodulator

- Digital communication networks, that is a network designed expressly for transmitting information in digital form to achieve much higher data transfer rate. An eg. Of such network is ISDN.

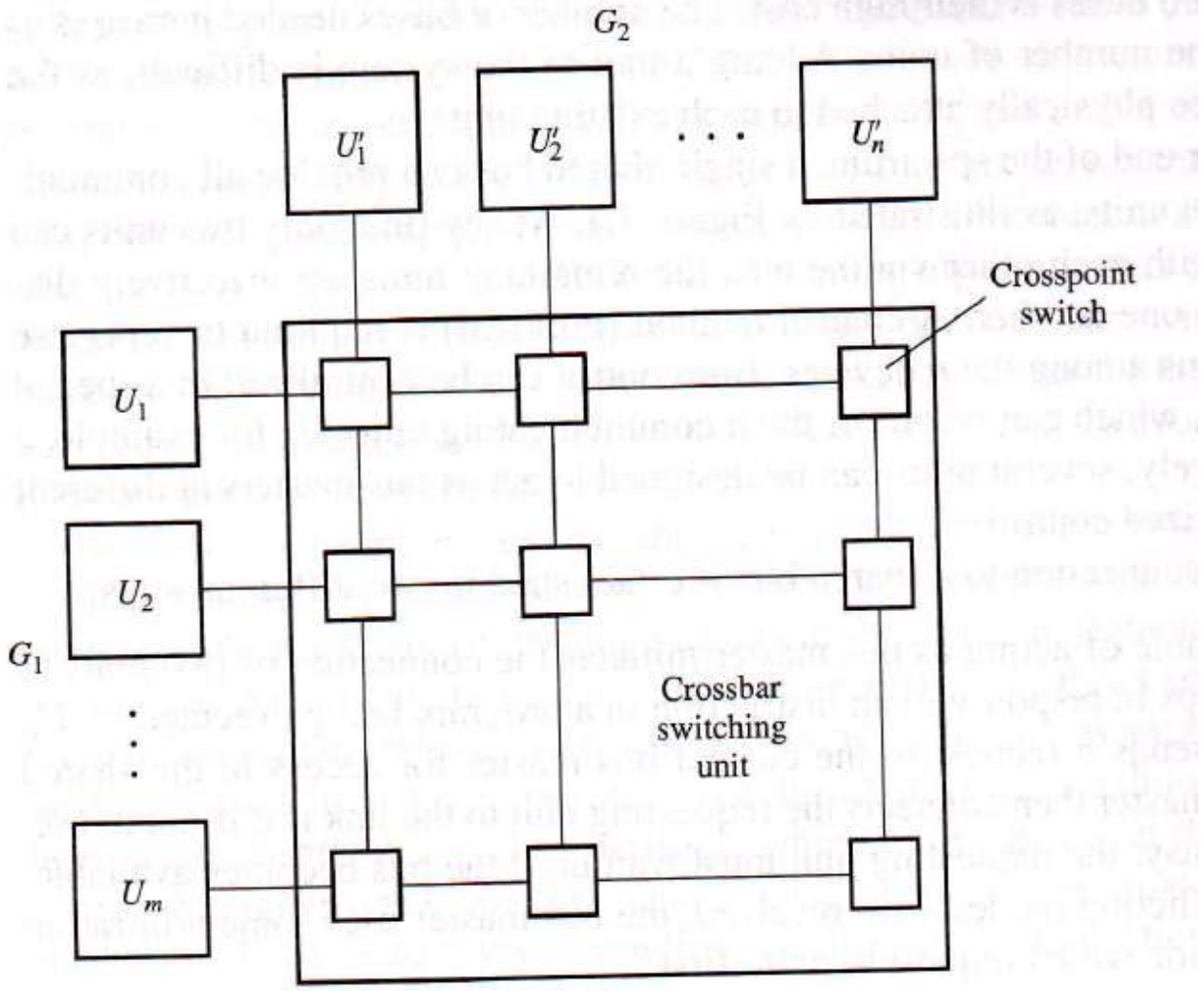
- Digital communication can be done by making use of interconnected computer which is known as computer network.

- Within a network data is transferred by making use of 3 techniques:
  - Circuit Switching
  - Message Switching
  - Packet Switching

- Network can be classified as
  - LAN
  - WAN

- Access with in a LAN can be done by making use of two access method
  - CSMA/CD
  - Token Passing

Crossbar Switching



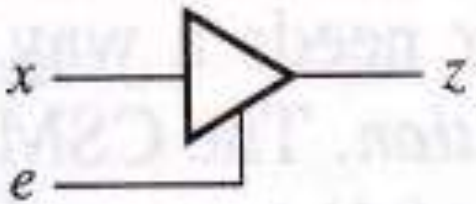
BUS Control

- Linear----Node Degree-----2
- Mesh----Node Degree-----4
- Ring----Node Degree-----2
- Star----Node Degree-----n-1
- Complete----Node Degree-----n-1
- Hypercube----Node Degree-----$\log_2 n$

Bus Interfacing

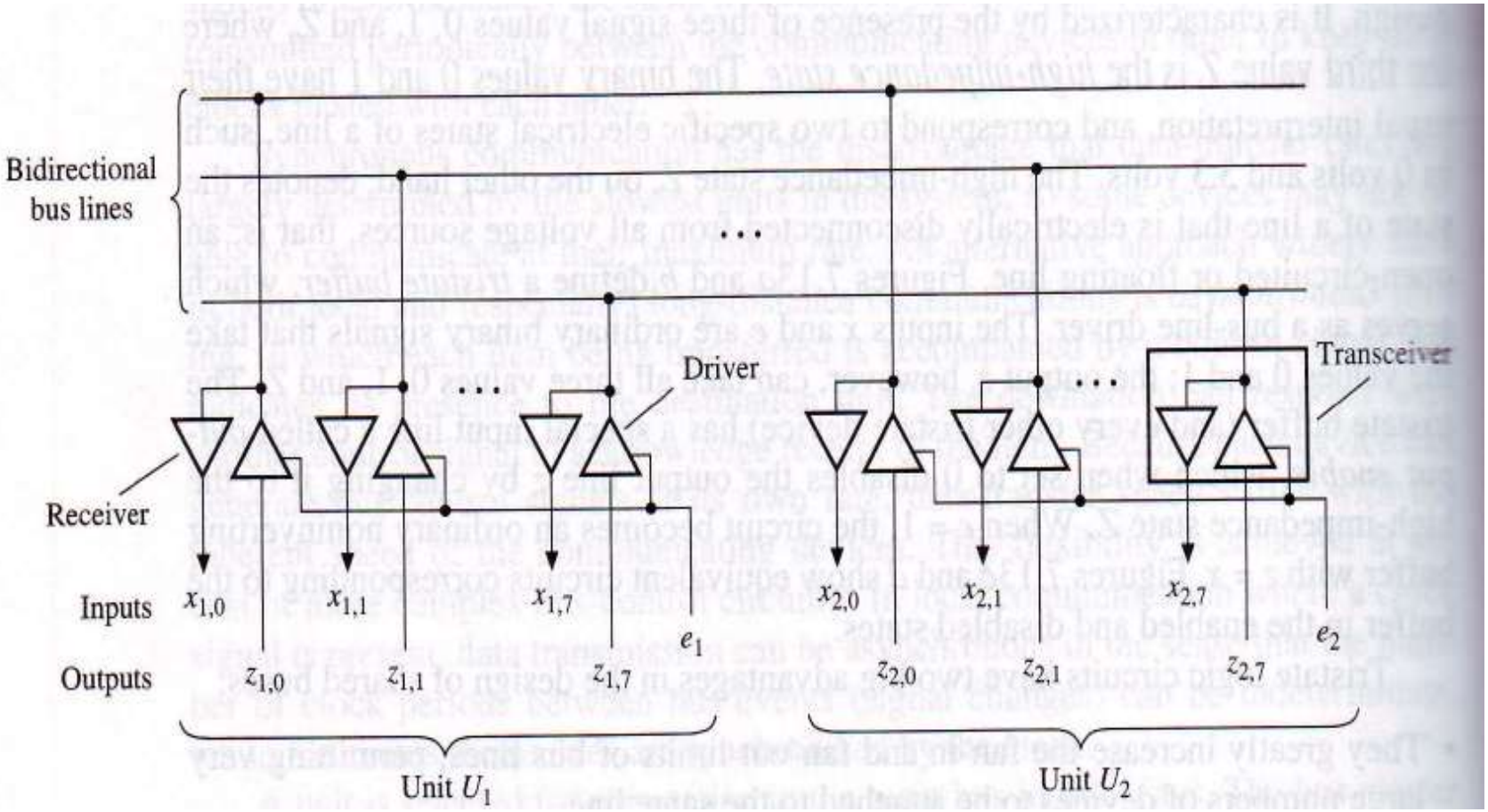
- A significant contributor to the cost of a bus is the number and the type of the circuits required to transfer signals to and from the bus.
- A special transistor circuit technology called tristate logic is often used in function design.
- The tristate logic is a three state gates that exhibits 3 state.
- The high impedance state behaves like an open circuit.

Symbol of a 3-state gate by using buffer:



Inputs		Outputs
x	e	z
0	1	0
1	1	1
0	0	Z
1	0	Z

Use of Tristate logic for Bus interfacing:



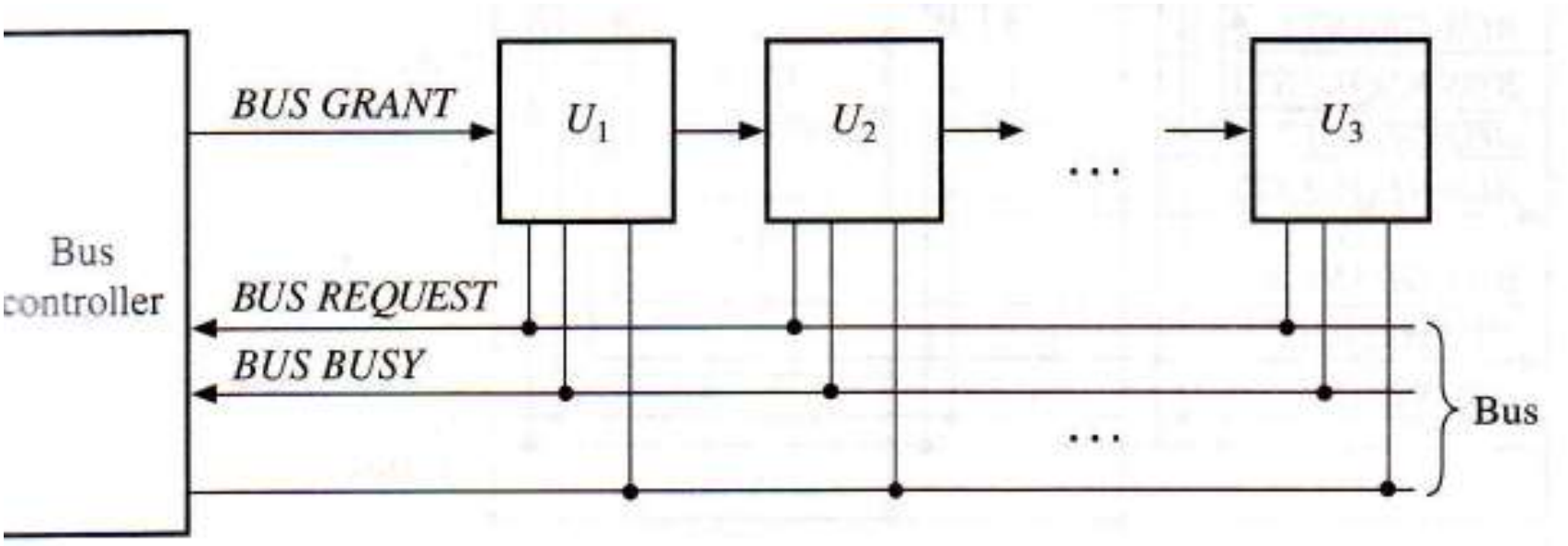
Data Transfer

- Synchronous Data Transfer
- Asynchronous Data Transfer

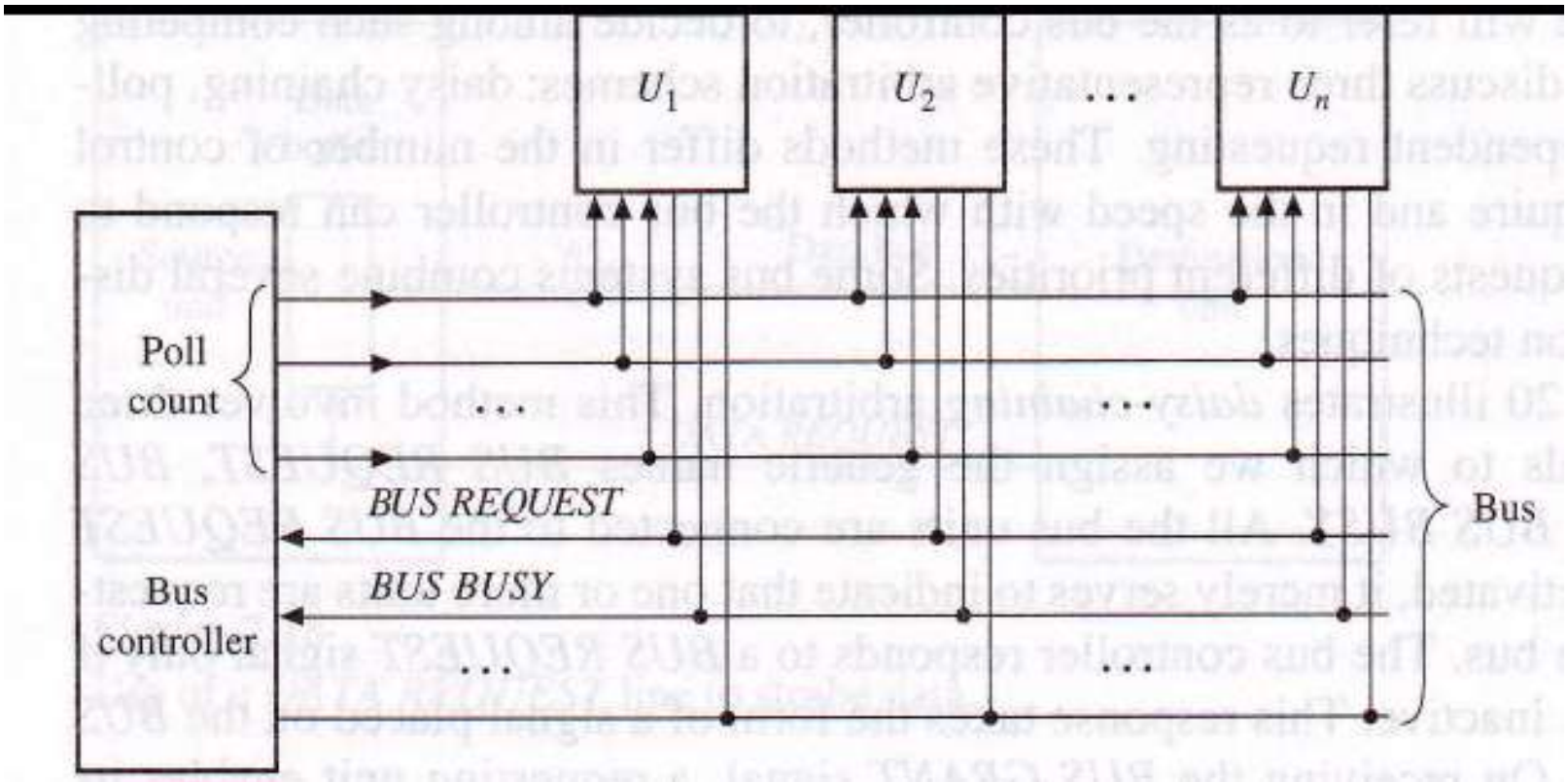
Bus Arbitration

- Daisy Chaining
- Polling
- Independent Requesting

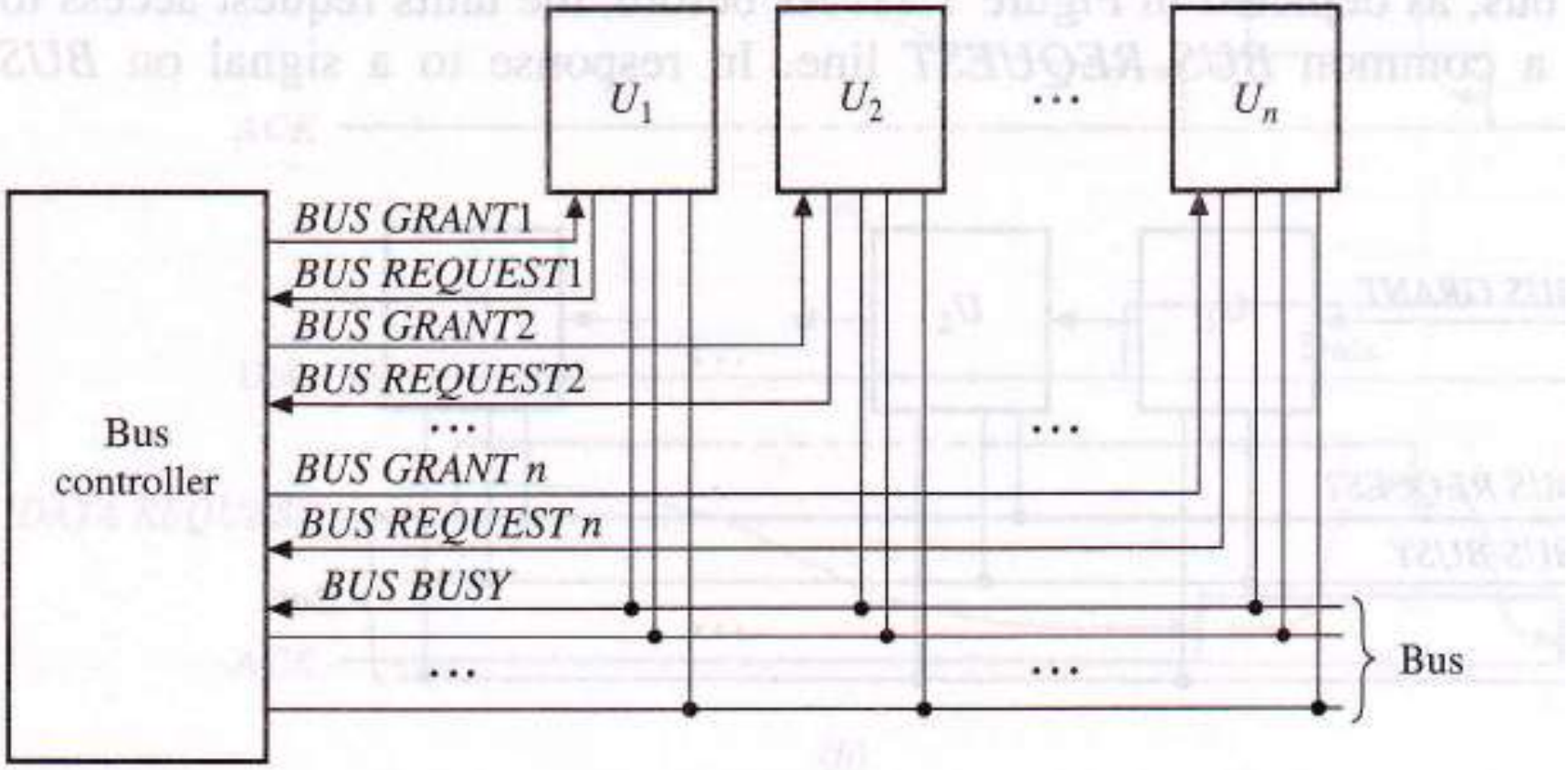
Daisy Chaining



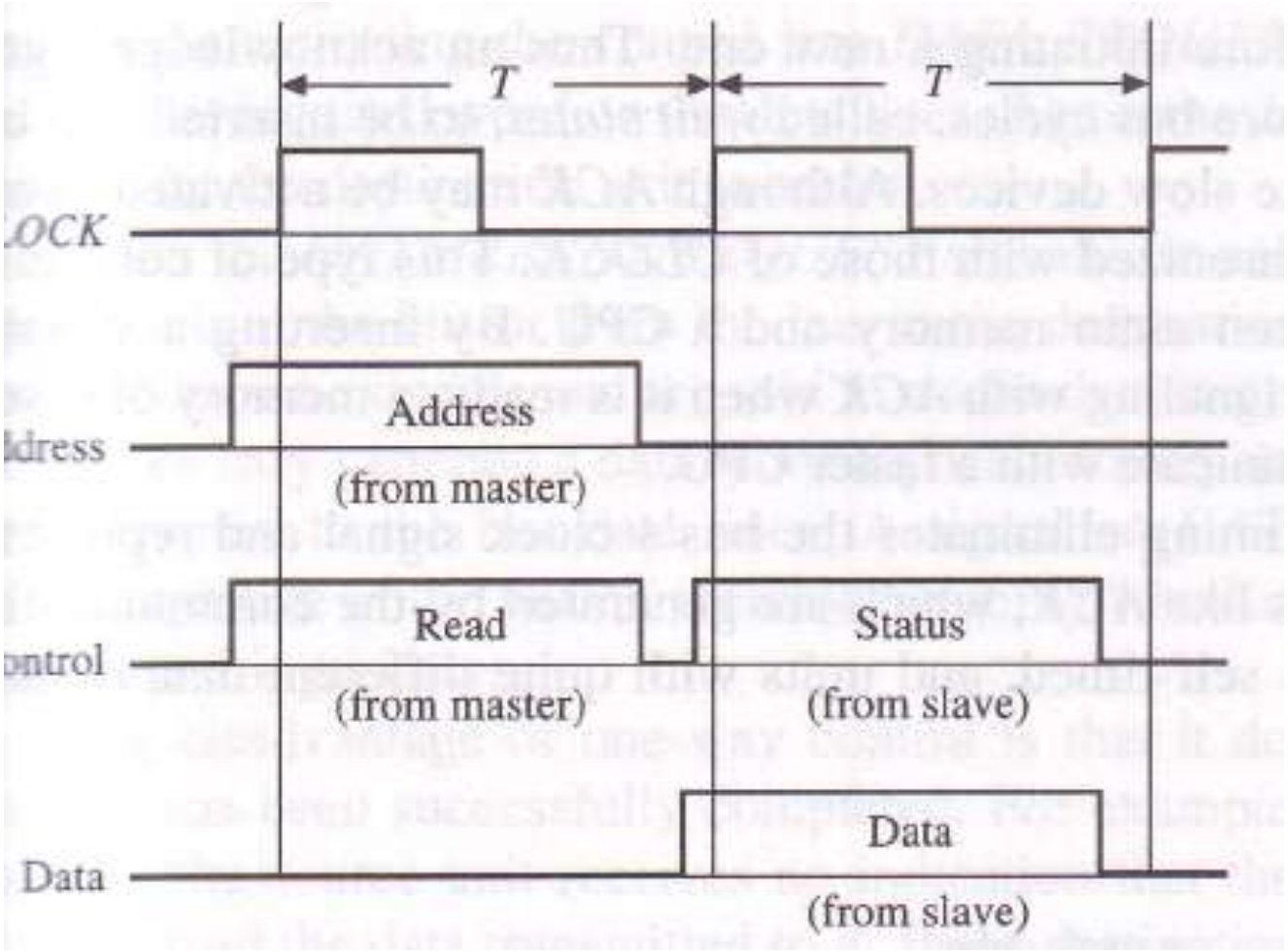
Polling



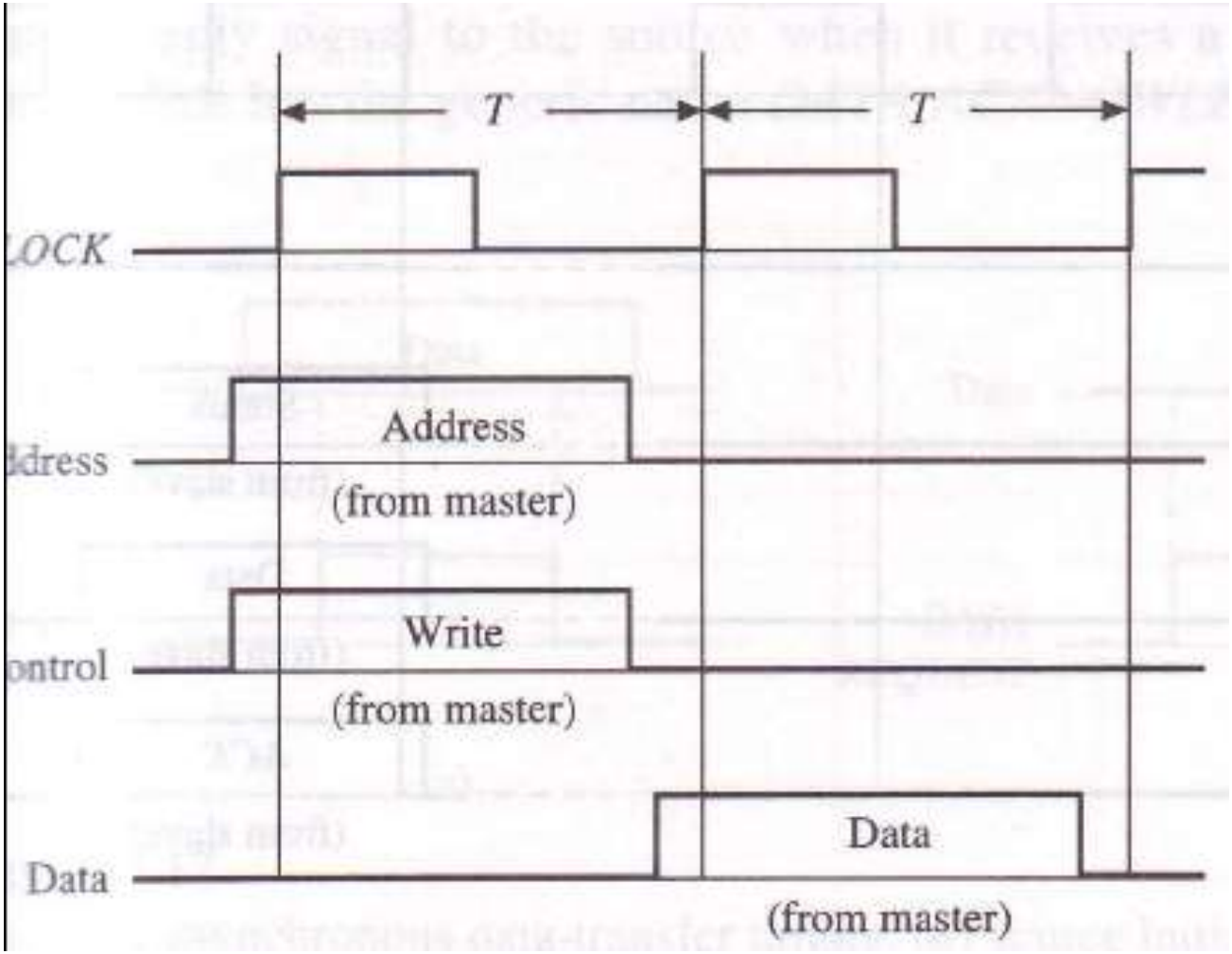
Independent Requesting



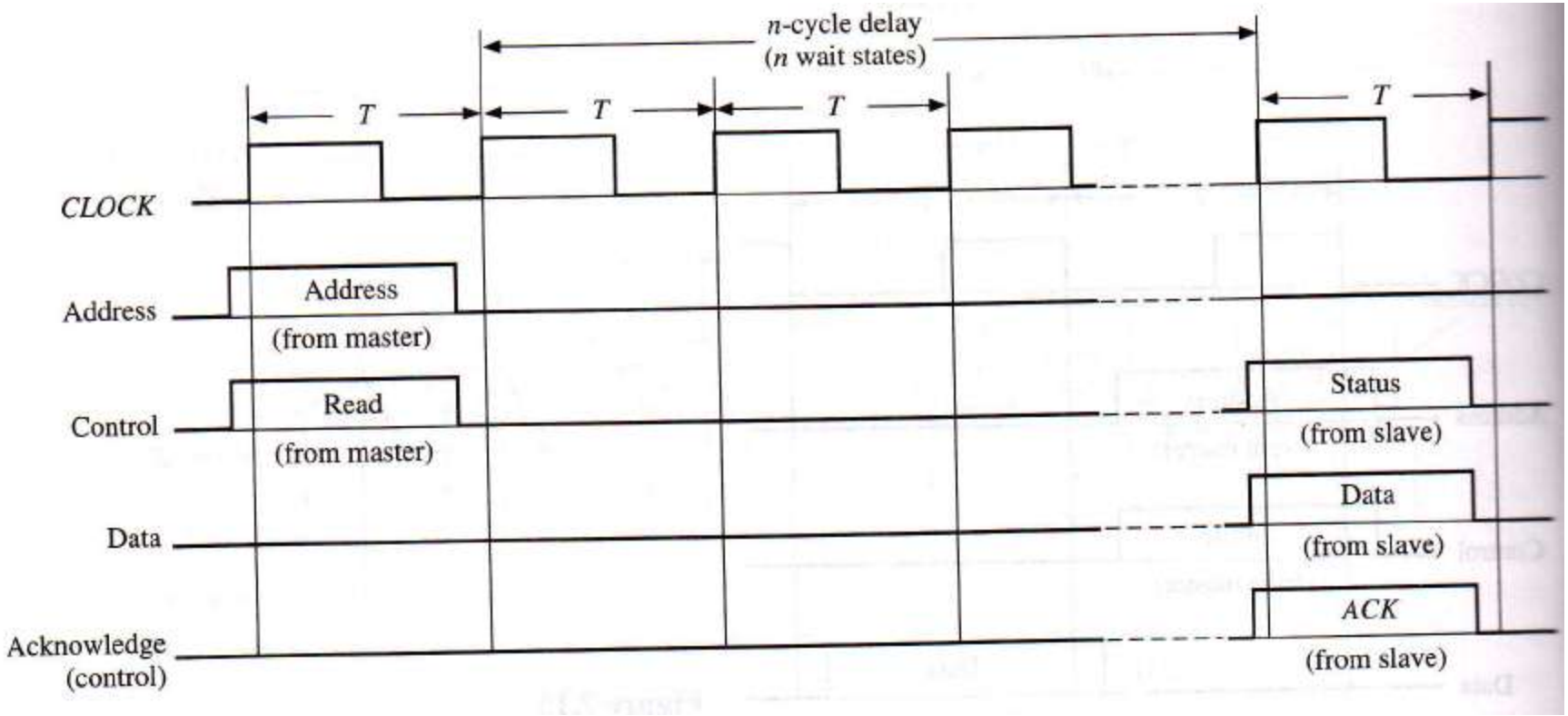
Synchronous Data Transfer for Read Operation:



Synchronous Data Transfer for Write Operation:



Synchronous Data Transfer for Read Operation With Wait States:



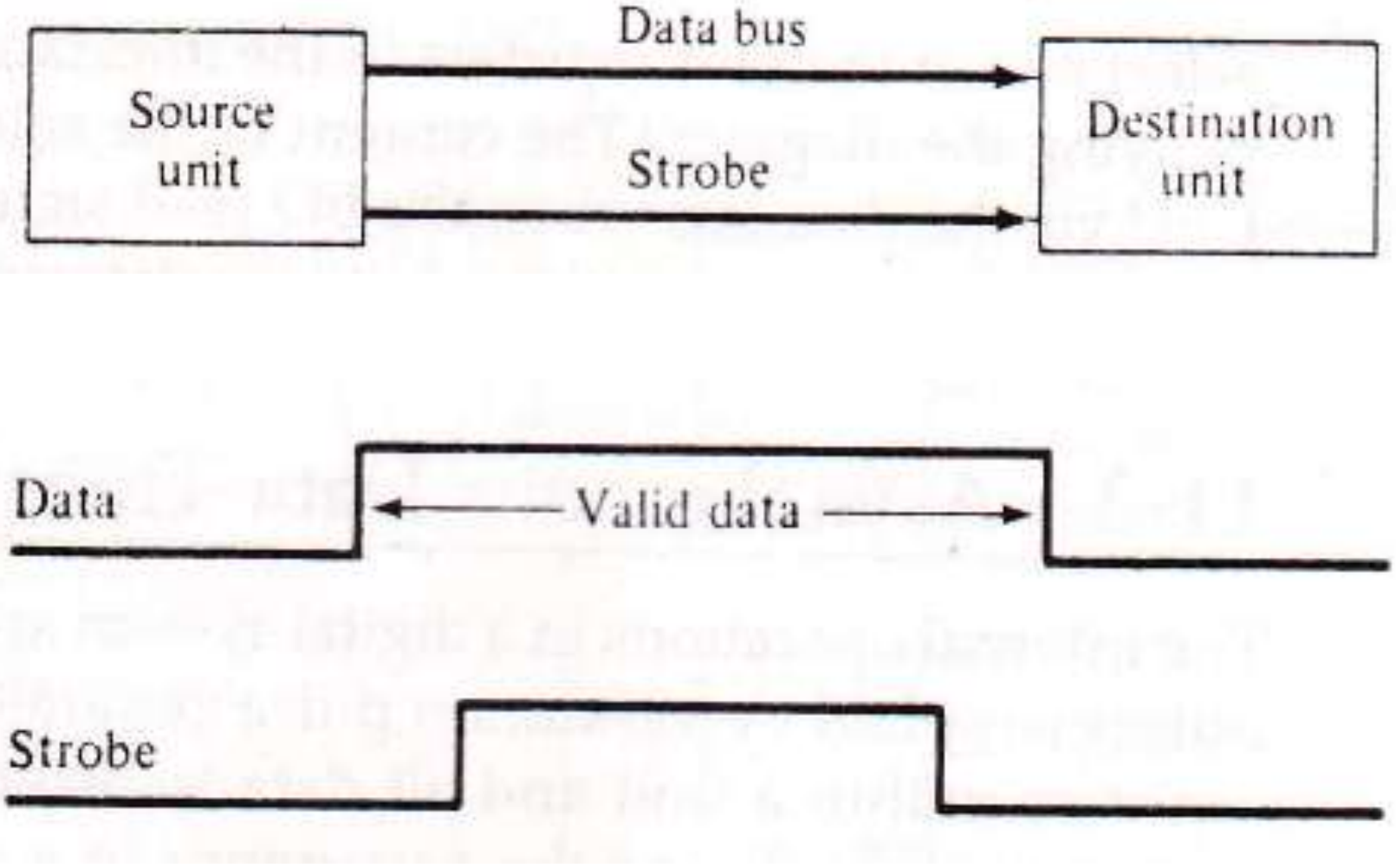
Asynchronous Data Transfer

- Strobe Control
- Handshaking

Strobe Control Contd…

- Source Initated Data Transfer
- Destination Initated Data Transfer

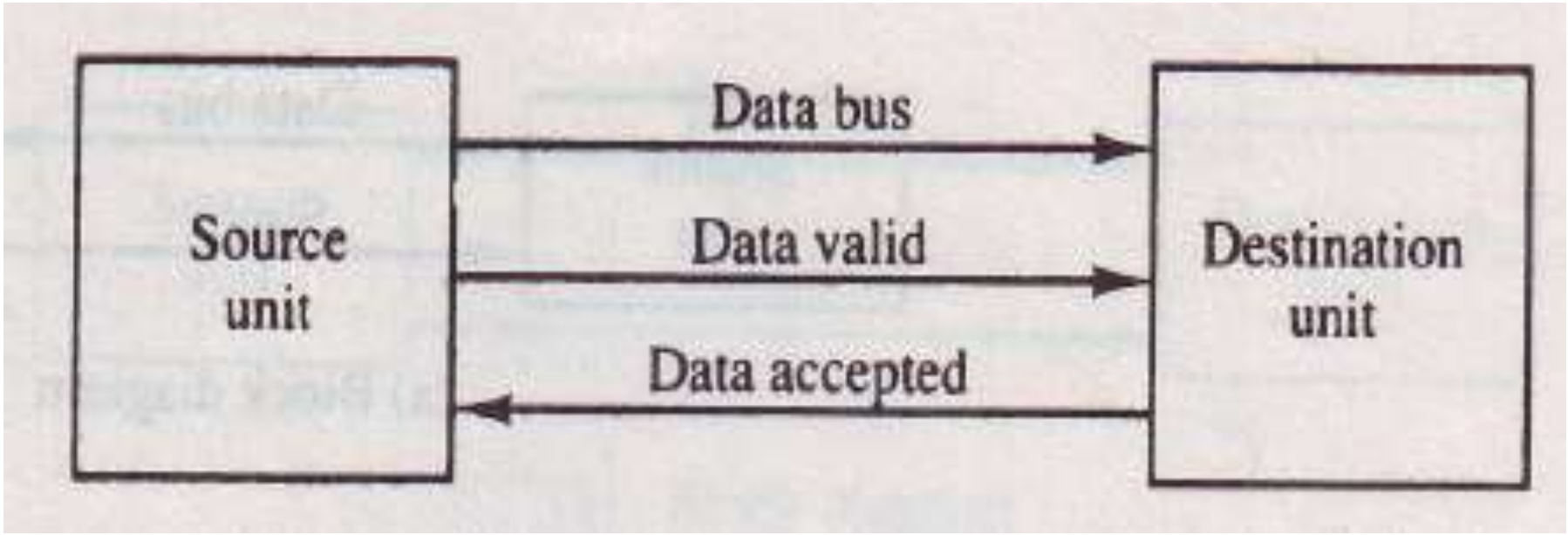
Source Initiated Data Transfer



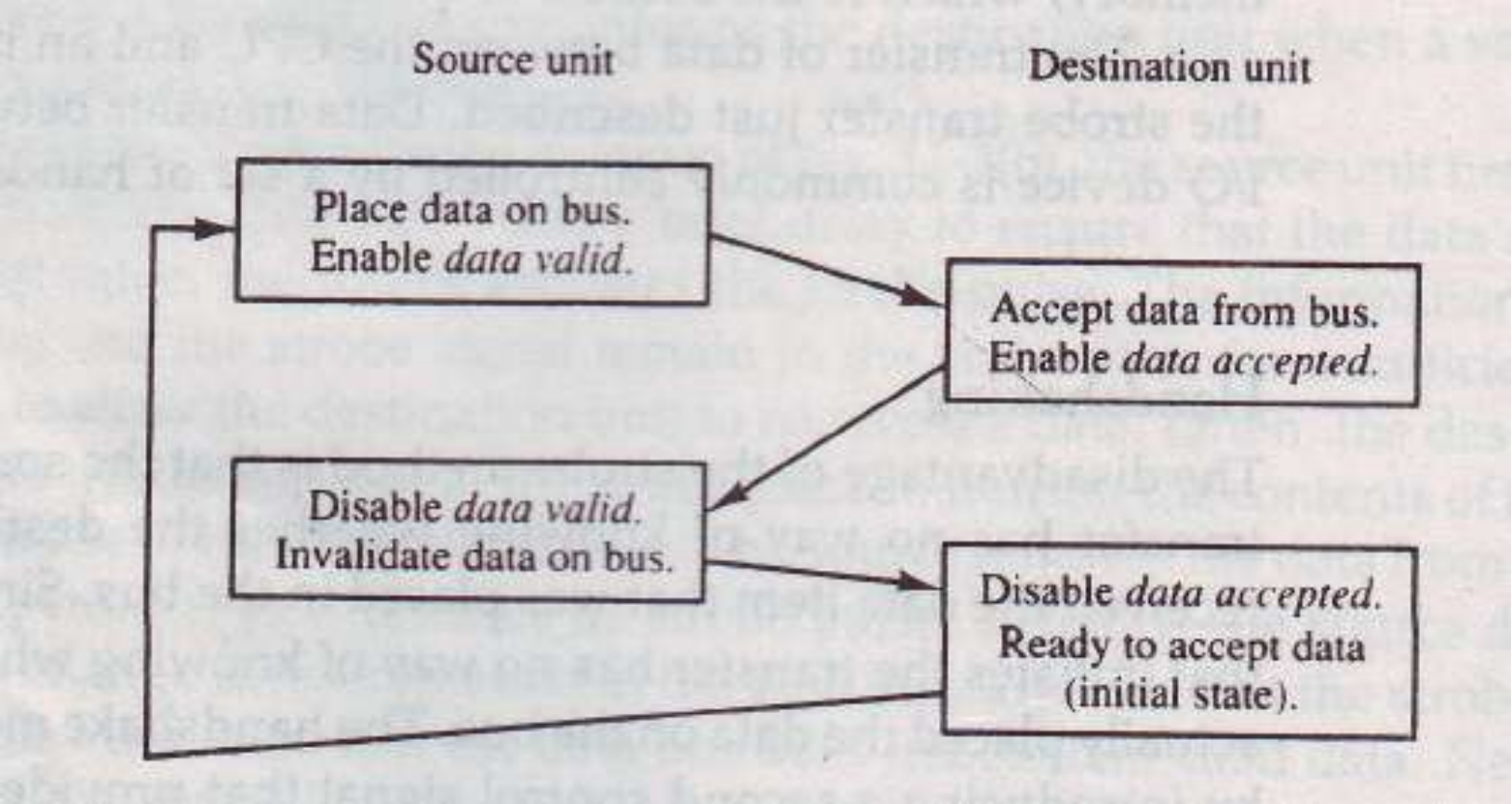
Handshaking

- Source Initated Data Transfer
- Destination Initated Data Transfer

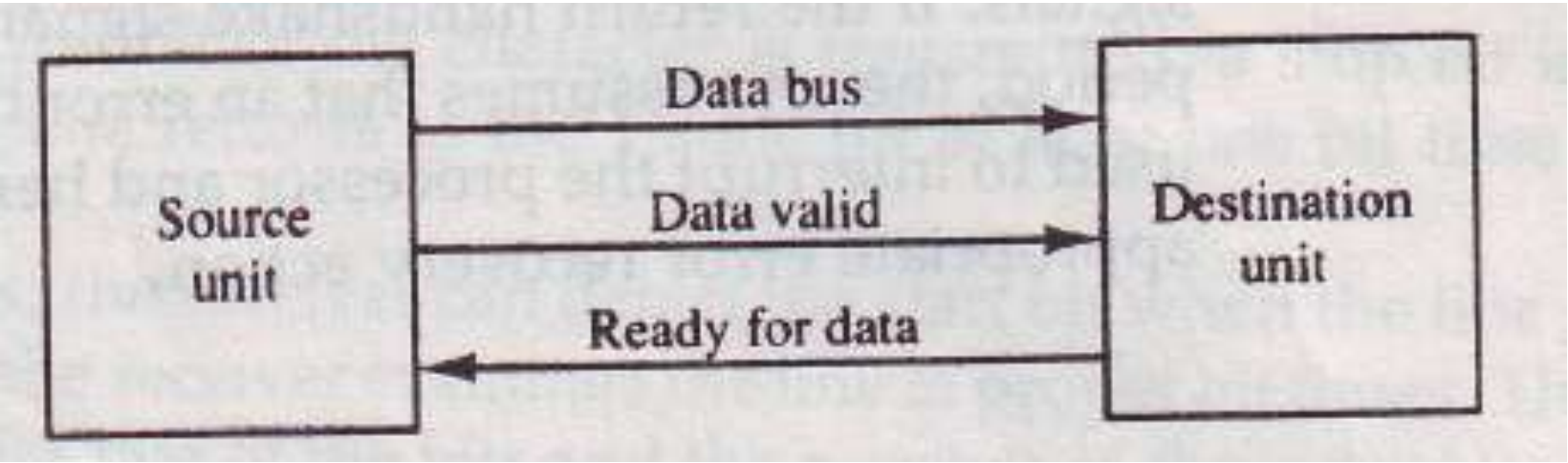
Source Initiated Data Transfer



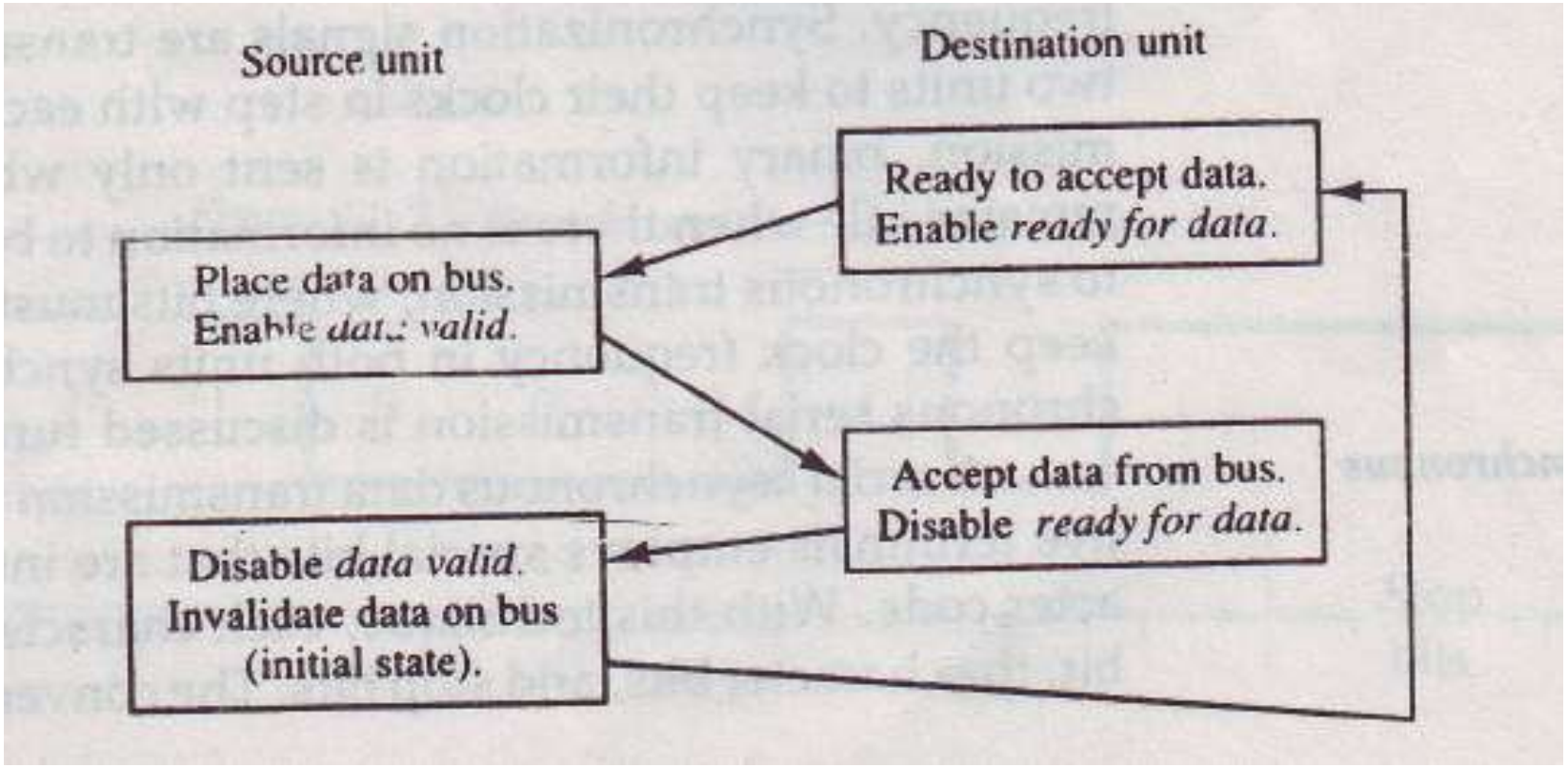
Source Initiated Data Transfer Contd…



Destination Initiated Data Transfer



Destination Initiated Data Transfer Contd…



How Data is transferred between 2 Units:

- Parallel Data Transmission
- Serial Data Transmission
  - Asynchronous Data Transmission
  - Synchronous Data Transmission

I/O Control Method

- Programmed I/O
- Interrupt Initiated I/O
- DMA

Programmed I/O

- There are 3 ways
  - Use 2 separate buses
  - Use 1 common bus for both memory & I/O but have separate control lines. (Isolated I/O)
  - Use 1 common bus for both memory and I/O (Memory-Mapped I/O)

Interrupt Initiated I/O

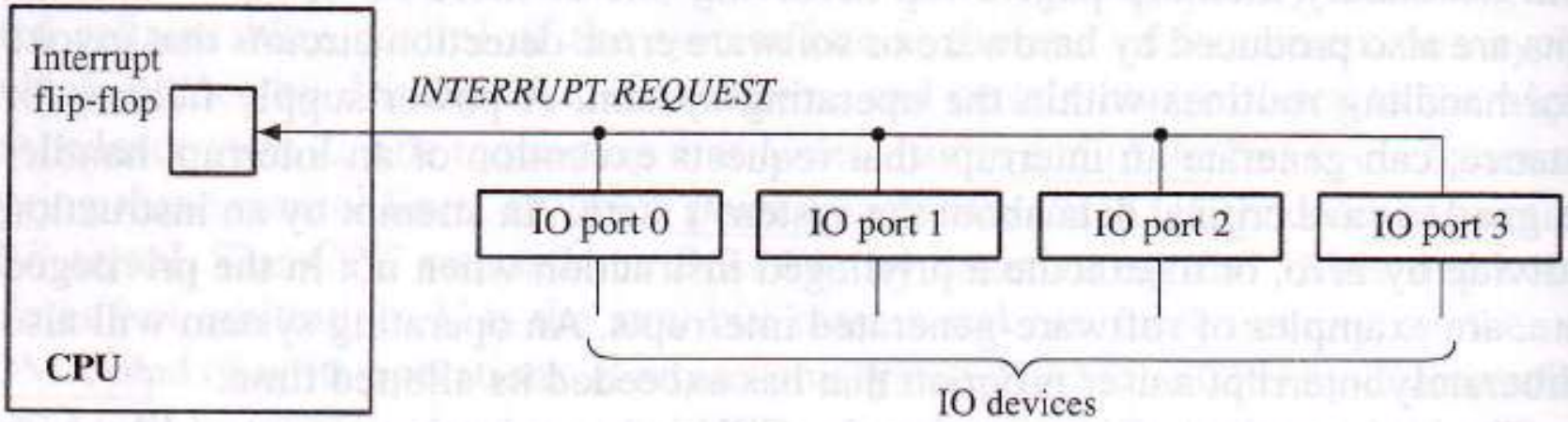
- Interrupt is an exceptional event that occurs during the execution of the program.
- While an interrupt occurs then CPU temporarily transfer the control from its current program to an interrupt handling program which is known as interrupt handler.
- The basic method of interrupting the CPU by activating it's control line named INTERRUPT REQUEST.

Interrupt Initiated I/O Contd…..

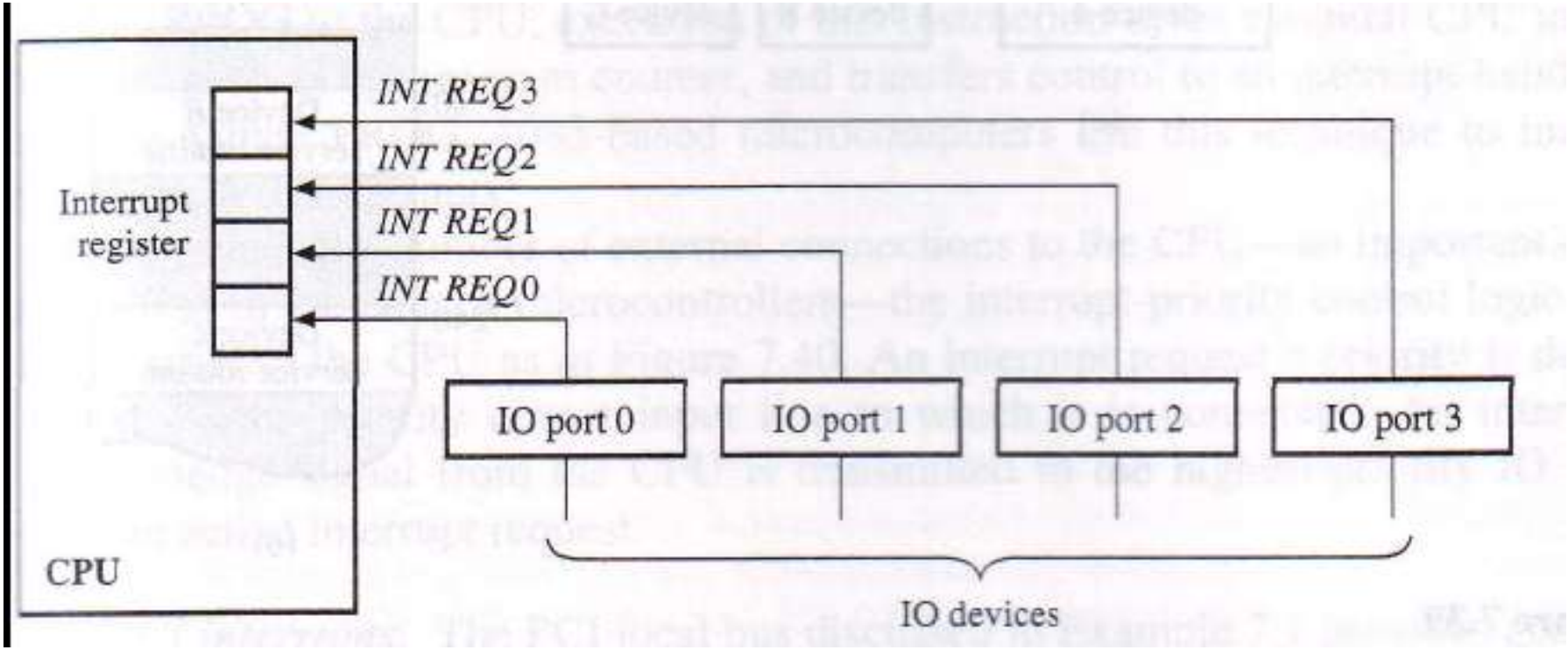
The CPU responds to an interrupt request by transfer a control to an interrupt handler . The following steps are taken:

- The CPU identifies the source of the interrupt.
- The CPU obtains the memory address of the required interrupt handler.
- According to that the PC and certain different registers are updated.

Interrupt Request By Using Single Line Interrupt System:



Interrupt Request By Using Multiple Line Interrupt System:



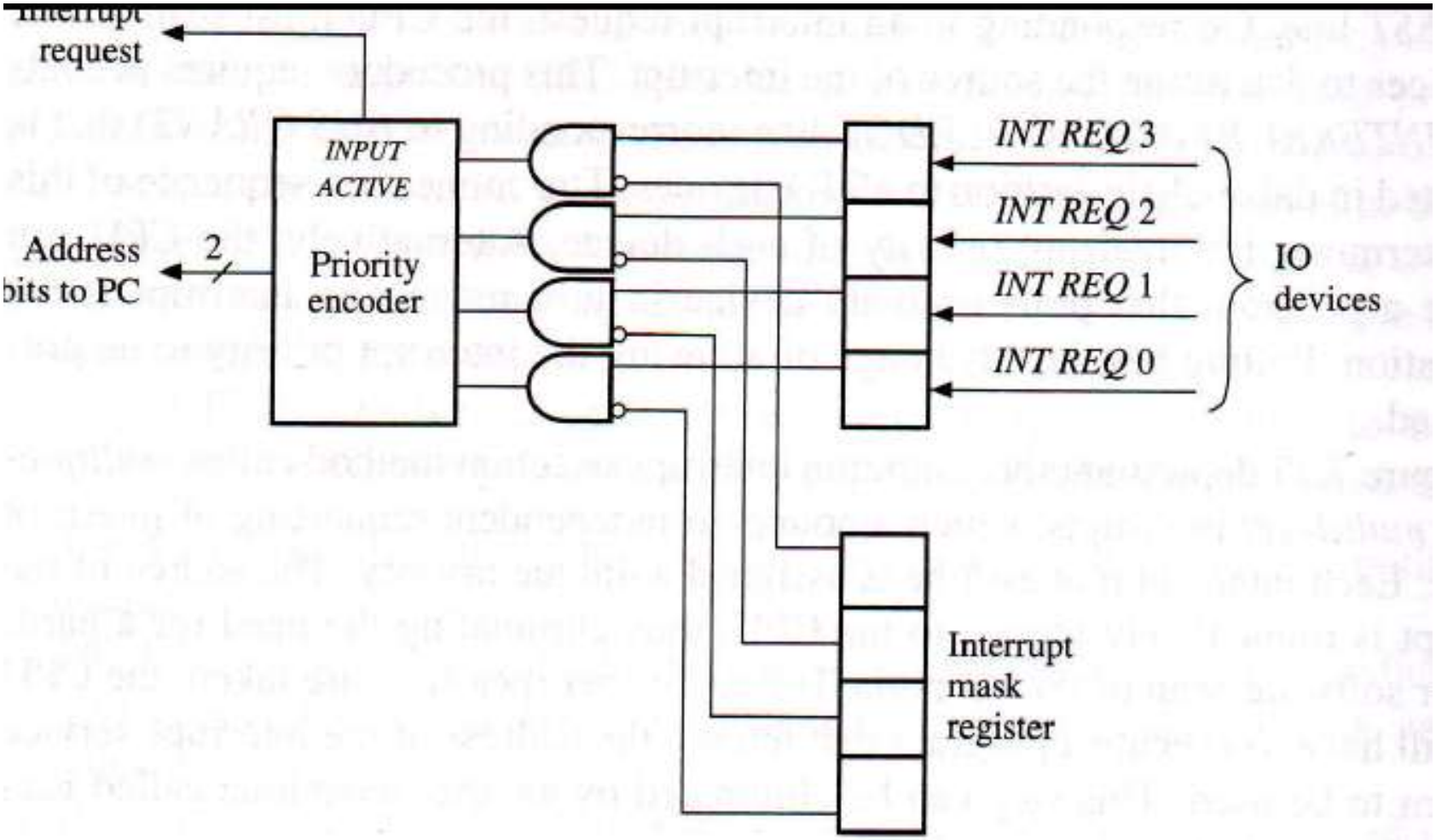
Interrupt Selection

- Daisy Chaining
- Polling
- Independent Requesting

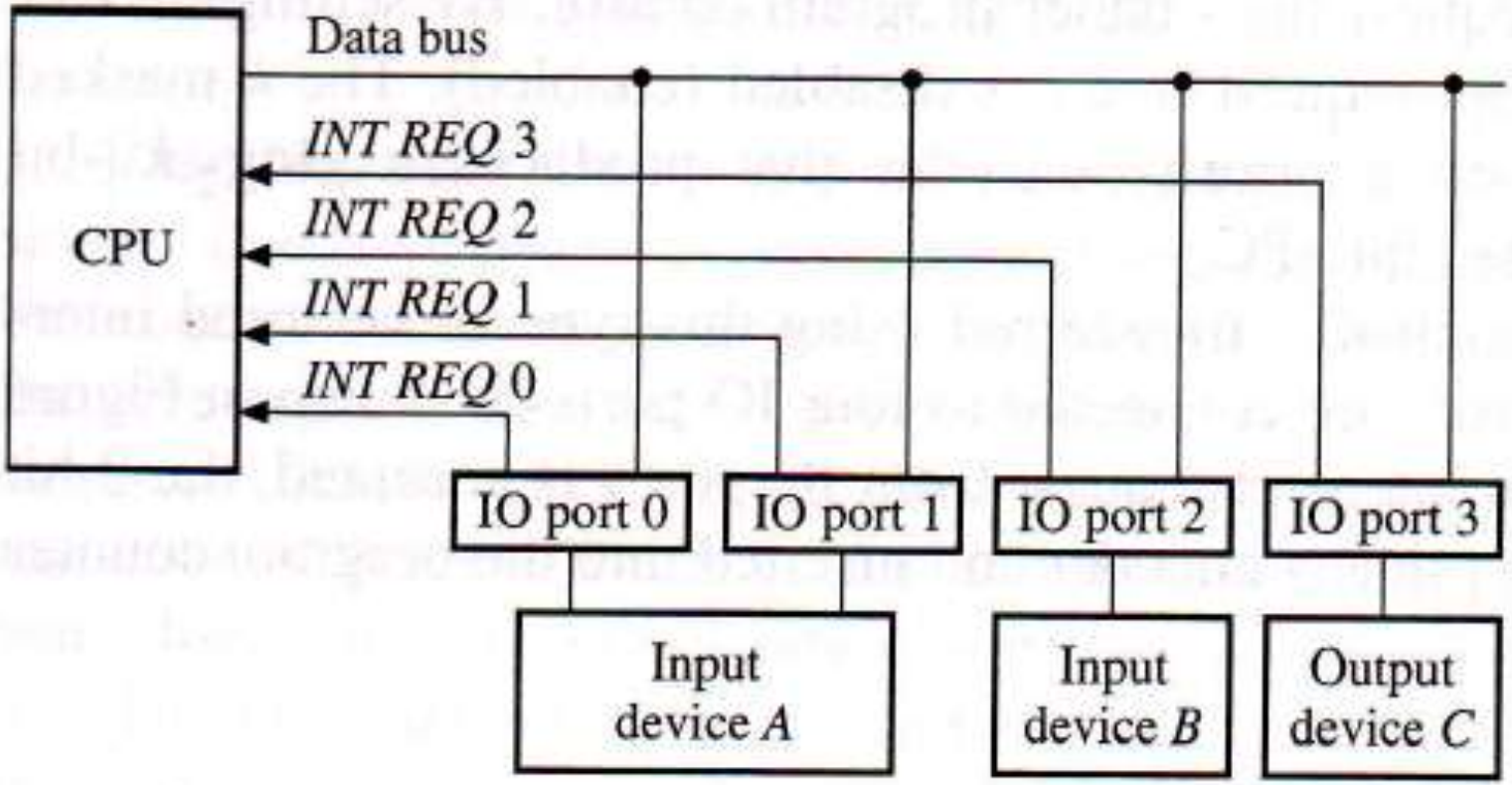
Vectored Interrupts

In case of Interrupt Initiated I/O, the interrupting device must supply the CPU with the starting address which is also known as interrupt vector of that program.

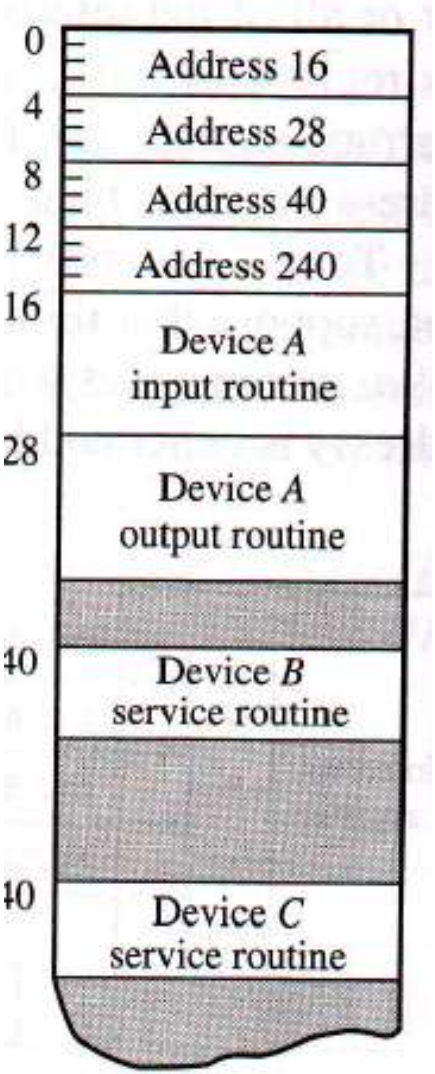
A Vectored Interrupt Scheme



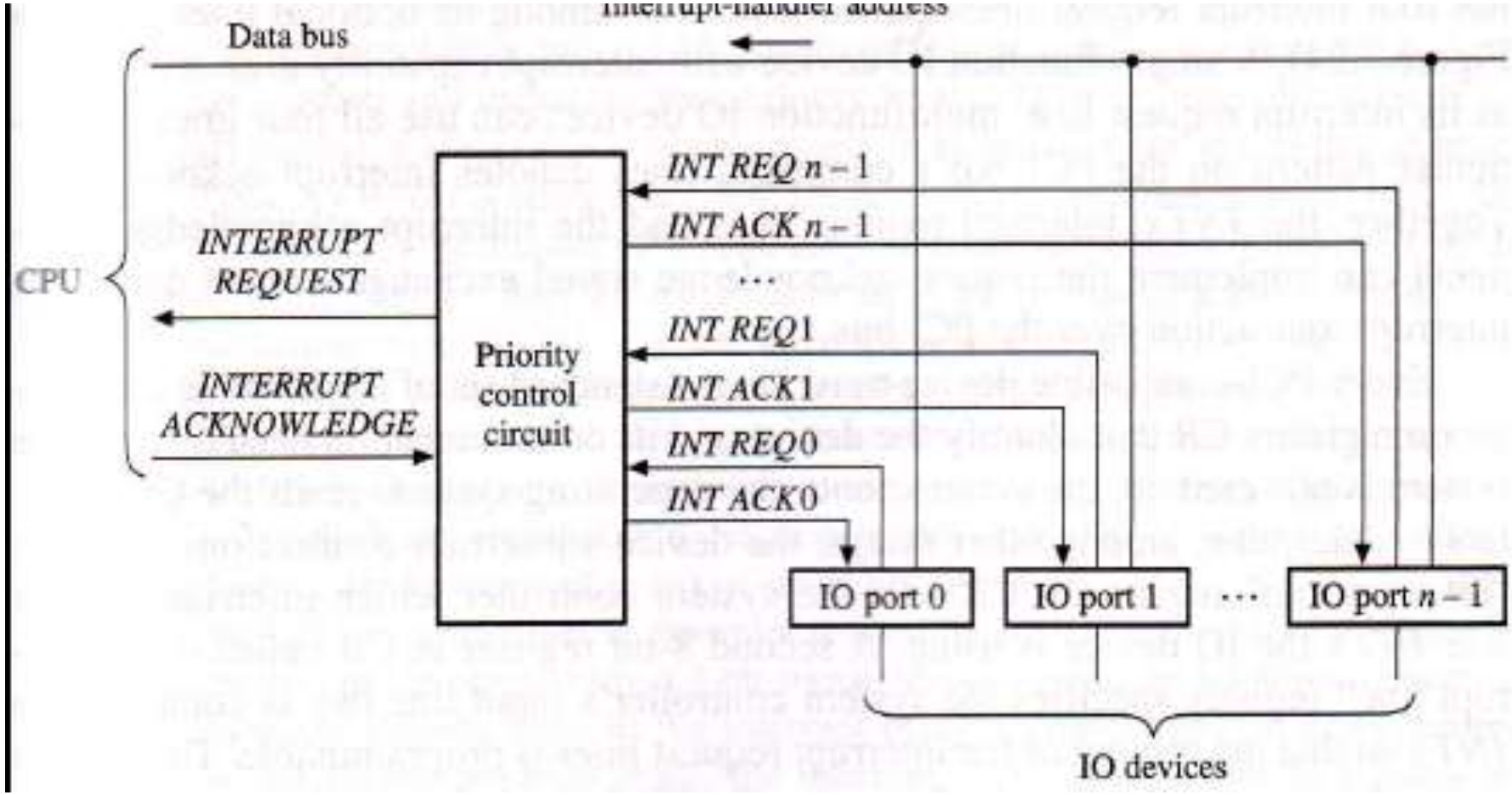
A Vectored Interrupt Scheme Contd…



A Vectored Interrupt Scheme Contd…

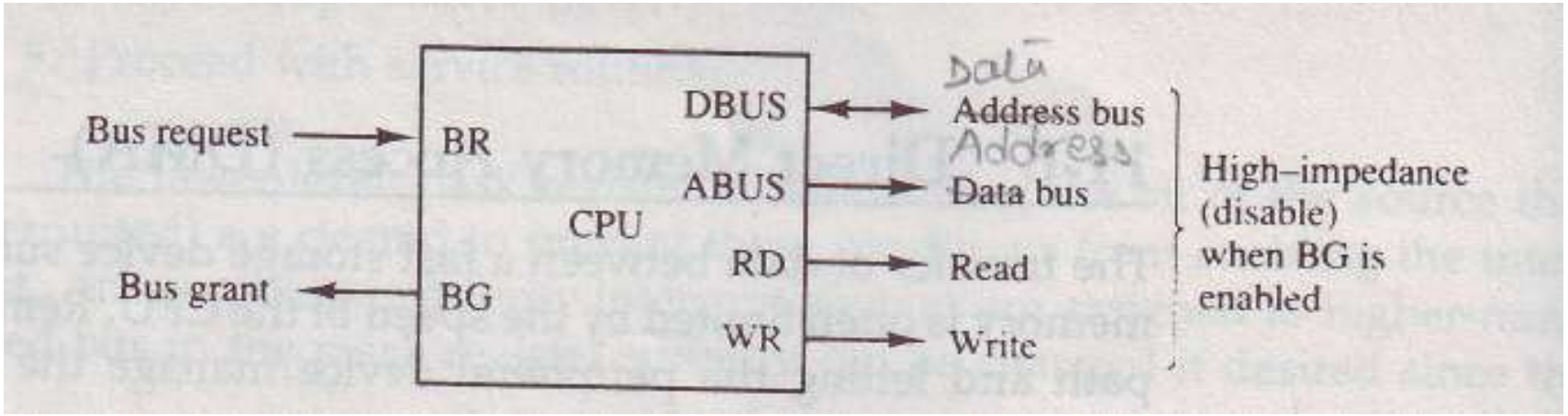


Implementation of Vectored Interrupt by Using Acknowledgement:

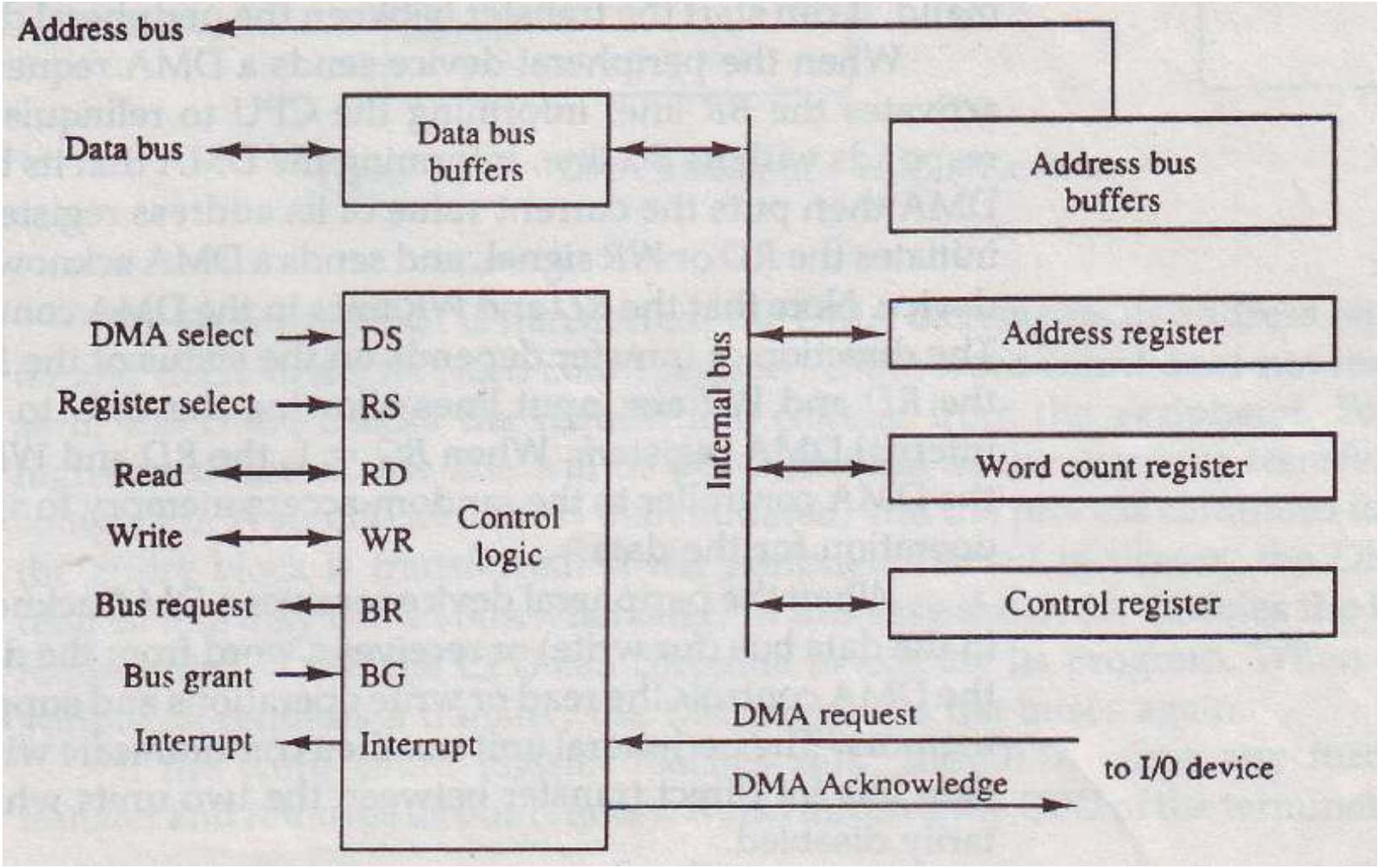


DMA (Direct Memory Access)

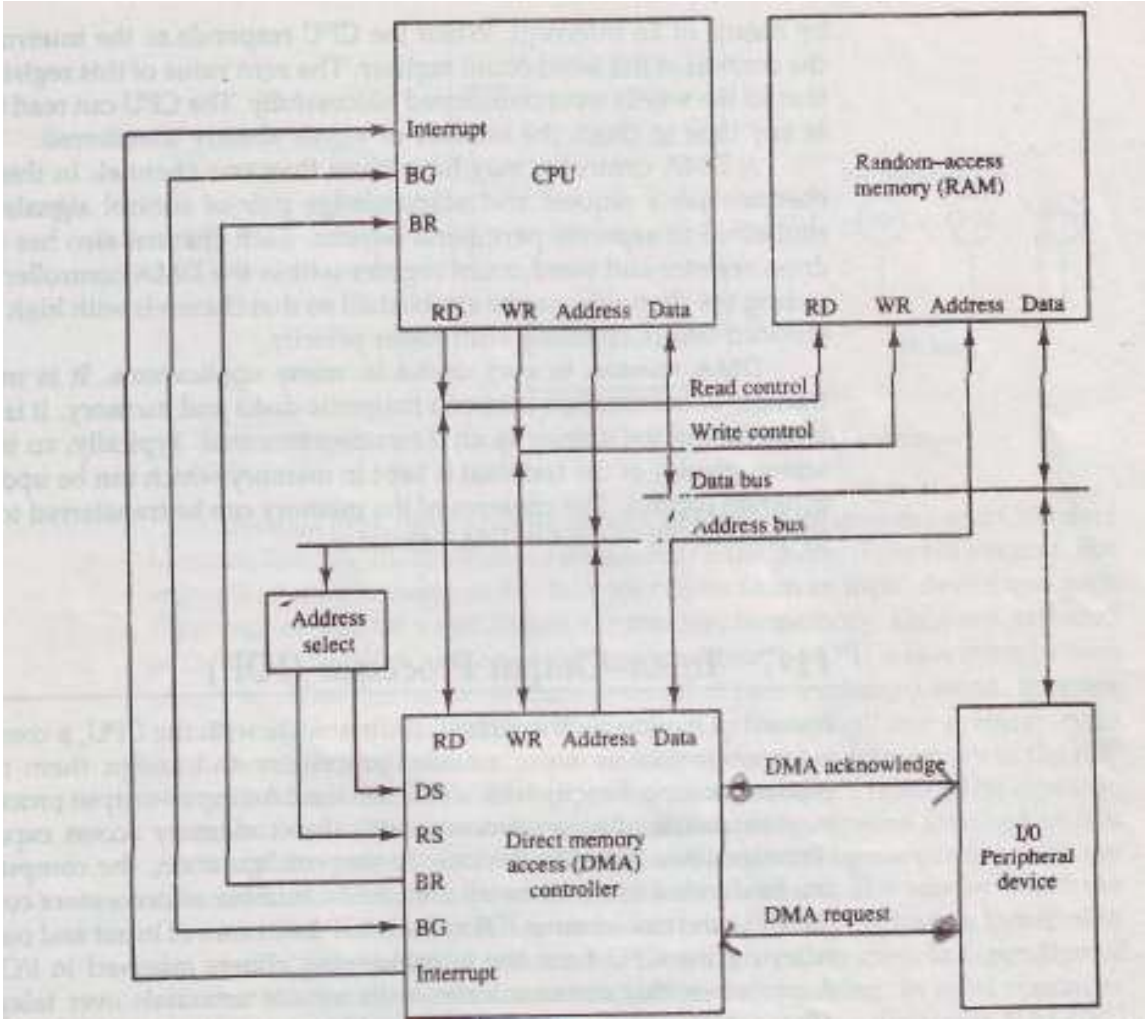
The transfer of data between a fast storage device such as magnetic disk and memory is often limited by the speed of the CPU. Removing CPU from the path and letting the peripheral device manage the memory buses directly would improve the speed of transfer. This transfer technique is called Direct Memory Access.


Bus request
BR
Bus grant
BG
CPU
DBUS
ABUS
RD
WR
Address bus
Data bus
Read
Write
High–impedance
(disable)
when BG is
enabled

Block Diagram of DMA Controller



DMA Transfer In A Memory System

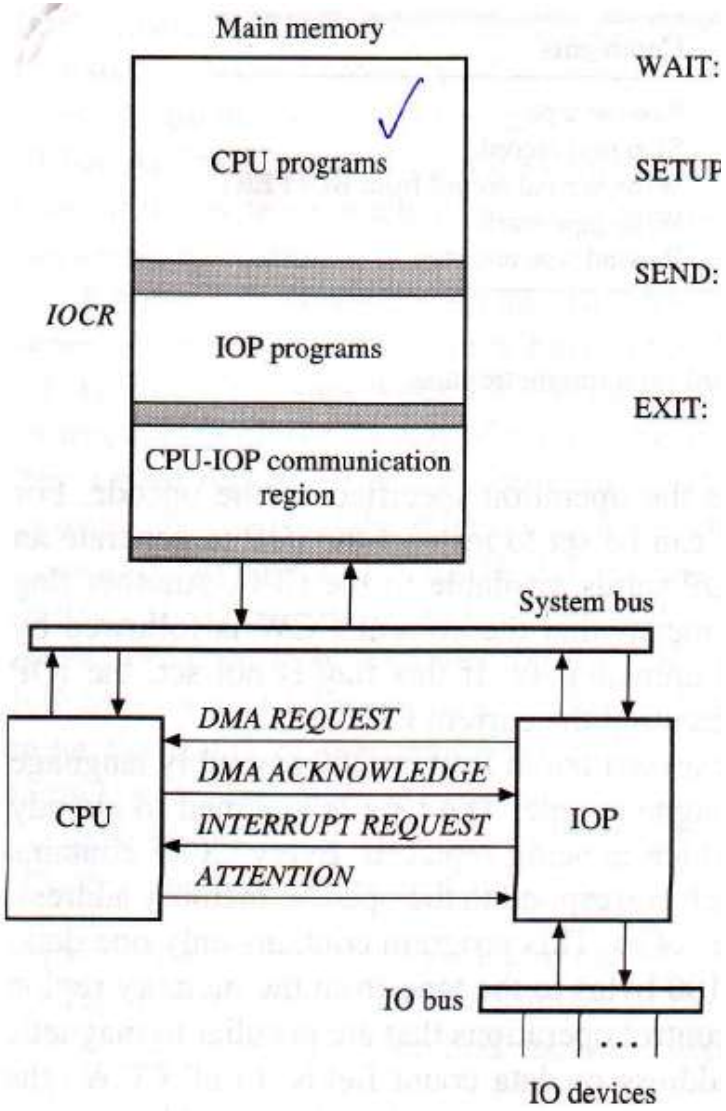


IO Processor

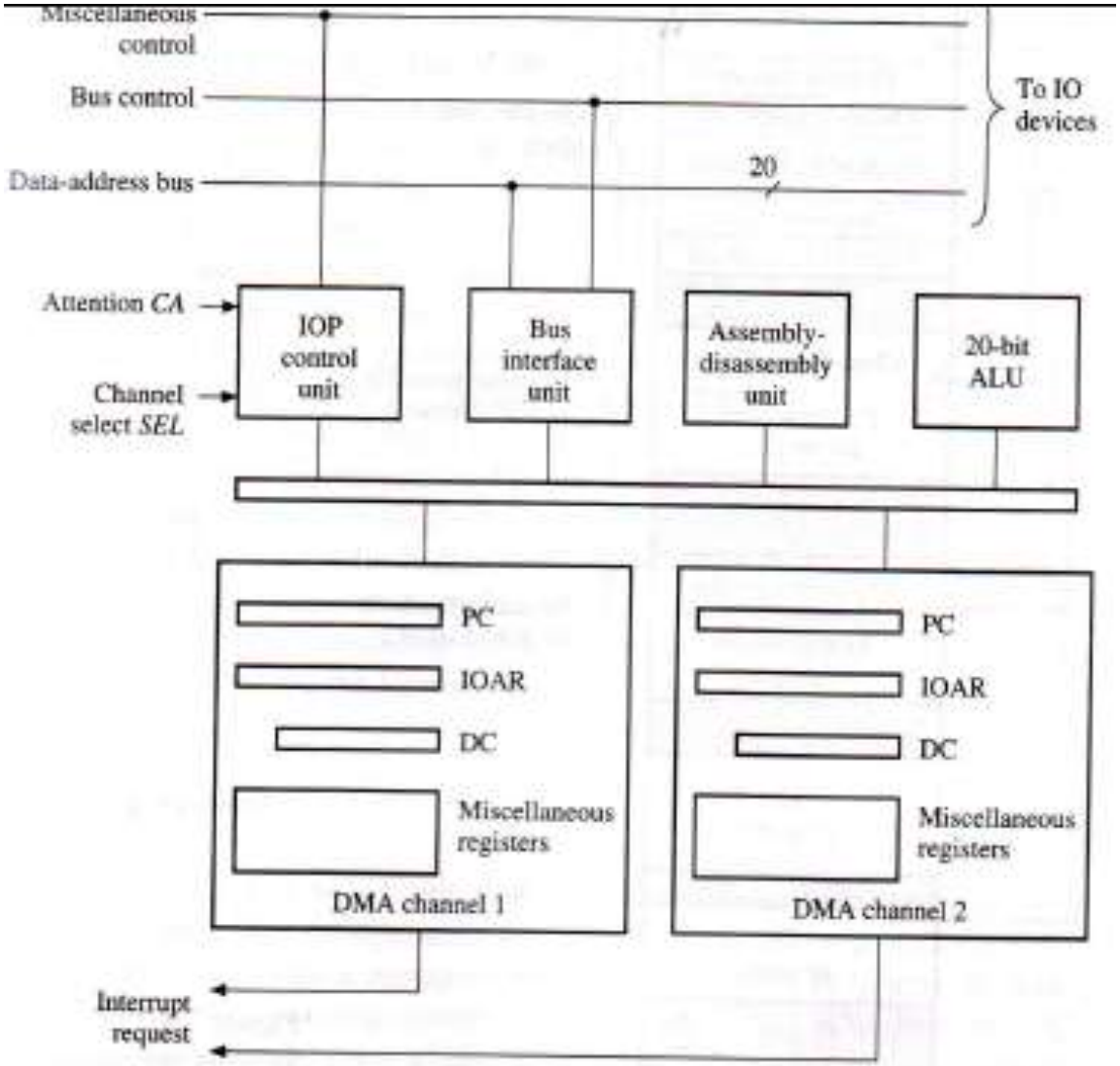
- An IO processor is an instruction set processor, with a more restricted instruction set.
- IO processor are primarily communication control units designed to link IO devices to a computer. They have also been called as Peripheral Processing Unit.
- In a computer with an IO processor, the CPU doesn't normally execute IO data-transfer instruction. Such instructions are stored in IO programs that are stored in Memory and are fetched and executed by the IO processor.

- The IO instruction executed by the IO processor are primarily associated with data transfer operations.
- The instructions executed by the IOP are called channel commands. They are of 3 types:
  - Data Transfer Instruction
  - Branch Instruction
  - I/O device control instruction

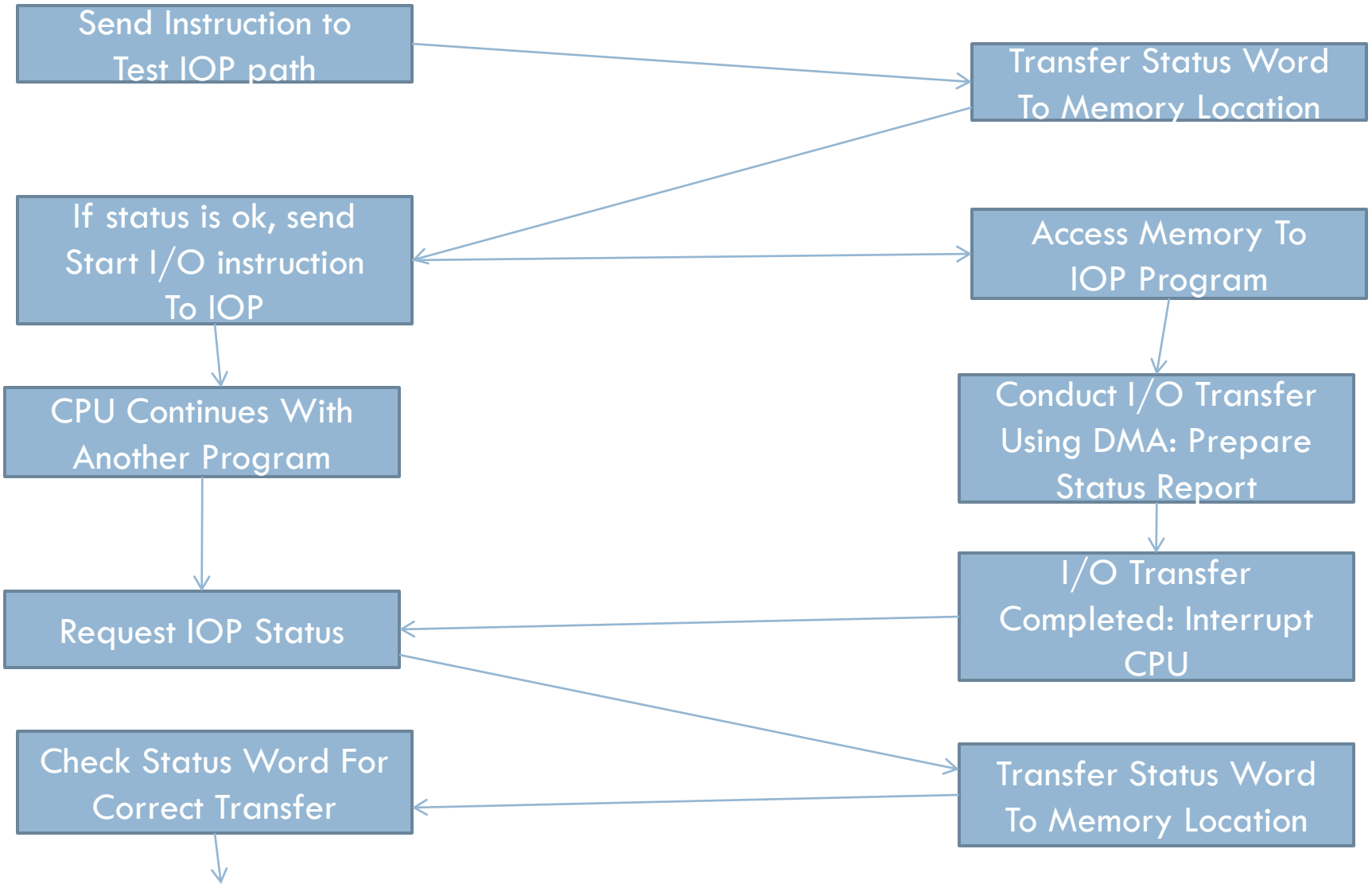
System Organization of Intel 8089 Processor:



Structure of the Intel 8089 IO Processor:



CPU-IOP Communication



Operating System

- An operating system is a program that act as a interface between the user and the computer hardware.

- Basic functions of Operating System
  - Process management
  - Memory management
  - File management
  - Device Management

Operating System Contd….

- Efficiency of operating system can be measured as:
  - Turn arround Time
  - Waiting Time
  - Throughput

- Thus we can say that an operating system is efficient iff turn arround time and waiting time is less and throughput is maximum.

Process Management

- ✓ The creation & deletion of process.
- ✓ The suspension & resumption of process
- ✓ The provision of mechanism for process synchronization & communication
- ✓ The provision of mechanism for deadlock handling

Memory Management

- Keep track of which memory are currently being used and by whom
- Decide which process are to be loaded into memory when memory space becomes available.
- Allocate & Deallocate memory space as needed.

File Management

- ✓ The creation & deletion of file
- ✓ The creation & deletion of directories
- ✓ The support of primitives for manipulating files and directories.
- ✓ The mapping of file onto the secondary storage.
- ✓ The backup of file on the stable storage media.

Device Management

- All the hardware devices also have to be managed by the operating system, it should activate them, control them, issue command to the device, handle error etc.

- It should also provide an interface between the device and the system so that it becomes eassy to use those devices.

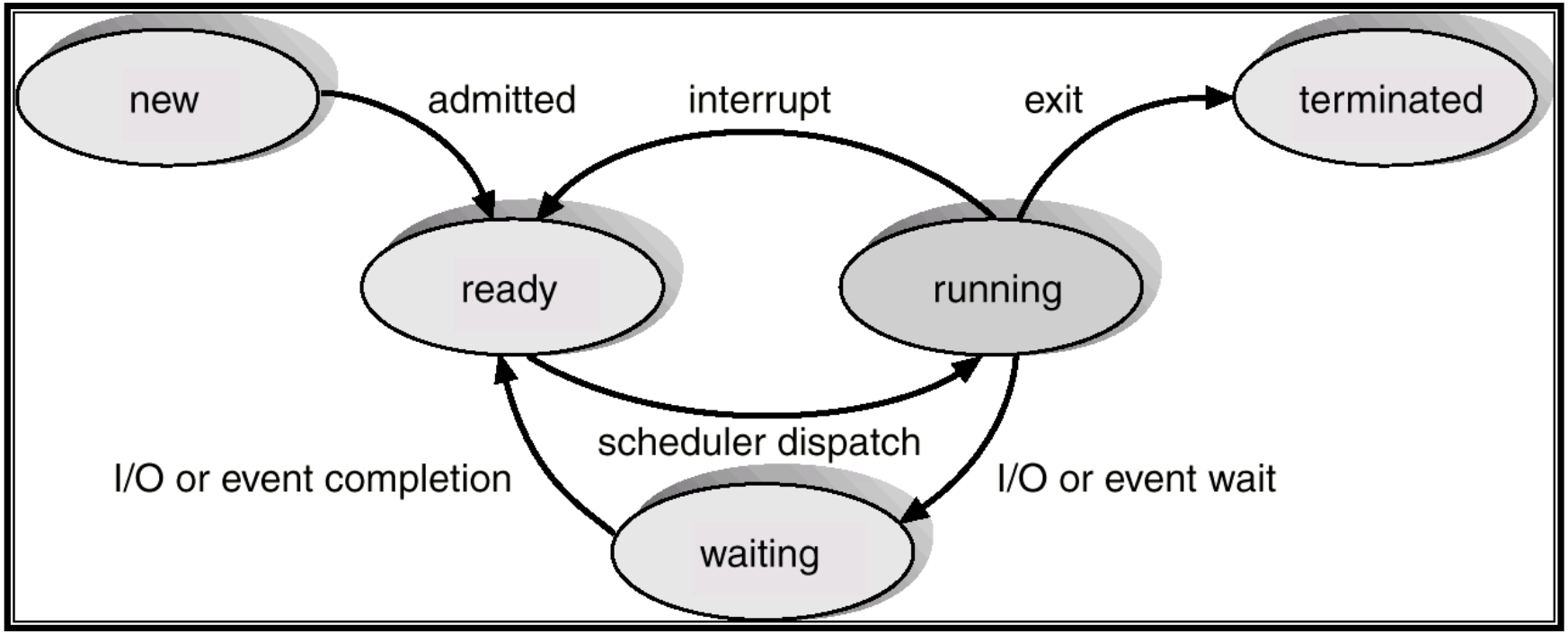
Kernel

The part of an operating system that resides in main memory and consist of most frequently used parts is termed as kernel.

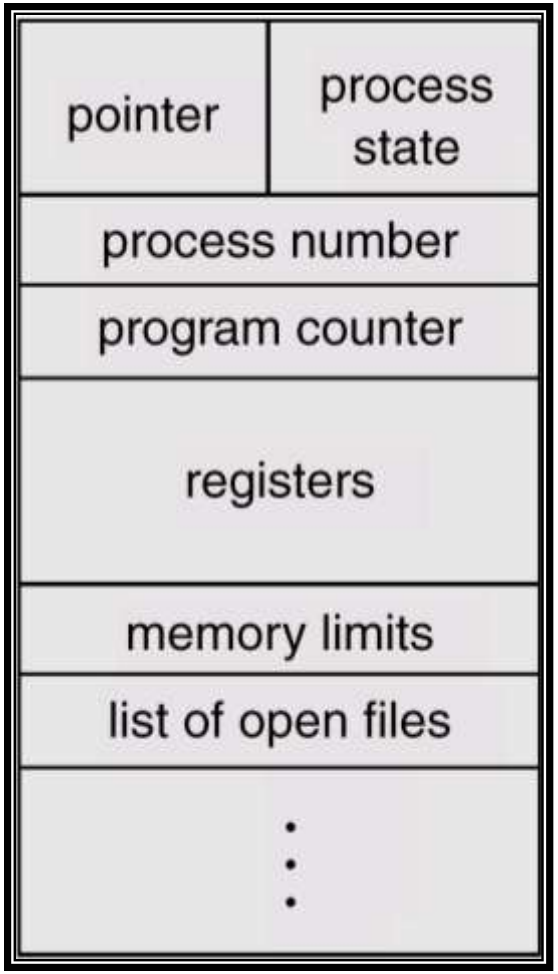
Processes

- A process is a program in execution.
- A program is a passive quantity and a process is an active quantity.
- As process executes, it changes the state:
  - New
  - Ready
  - Running
  - Waiting
  - Terminated

State of the Process



PCB (Process Control Block)



Deadlock

- A computer system has finite number of resources.
- In a multiprogramming environment several process may compete for a finite number of resources.
- A process request for the resources, if the resources are not available at that time, the process enters to a wait state.
- A deadlock state occurs when two or more processes are waiting indefinitely for an event that can be caused only by one of the waiting processes

- A deadlock may occur iff the 4 necessary condition will hold simultaneously
  - Mutual Exclusion
  - Hold & wait
  - No Preemption
  - Circular wait

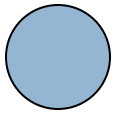
To prevent deadlock we ensure that atleast one of the condition never hold.

- **Mutual exclusion:** only one process at a time can use a resource.
- **Hold and wait:** a process holding at least one resource is waiting to acquire additional resources held by other processes.
- **No preemption:** a resource can be released only voluntarily by the process holding it, after that process has completed its task.
- **Circular wait:** there exists a set $\{P_0, P_1, \ldots, P_0\}$ of waiting processes such that P_0 is waiting for a resource that is held by P_1, P_1 is waiting for a resource that is held by

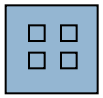
  $P_2, \ldots, P_{n-1}$ is waiting for a resource that is held by P_n, and P_0 is waiting for a resource that is held by P_0.

Resource Allocation Graph

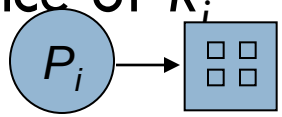
- Process



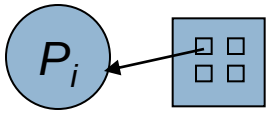
- Resource Type with 4 instances



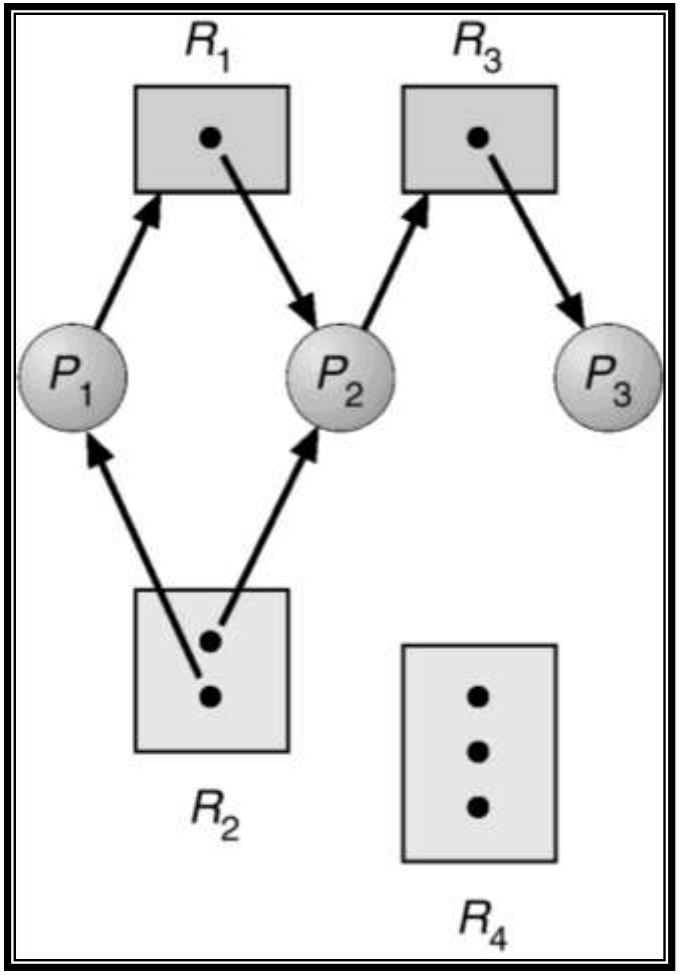
- P_i requests instance of R_i



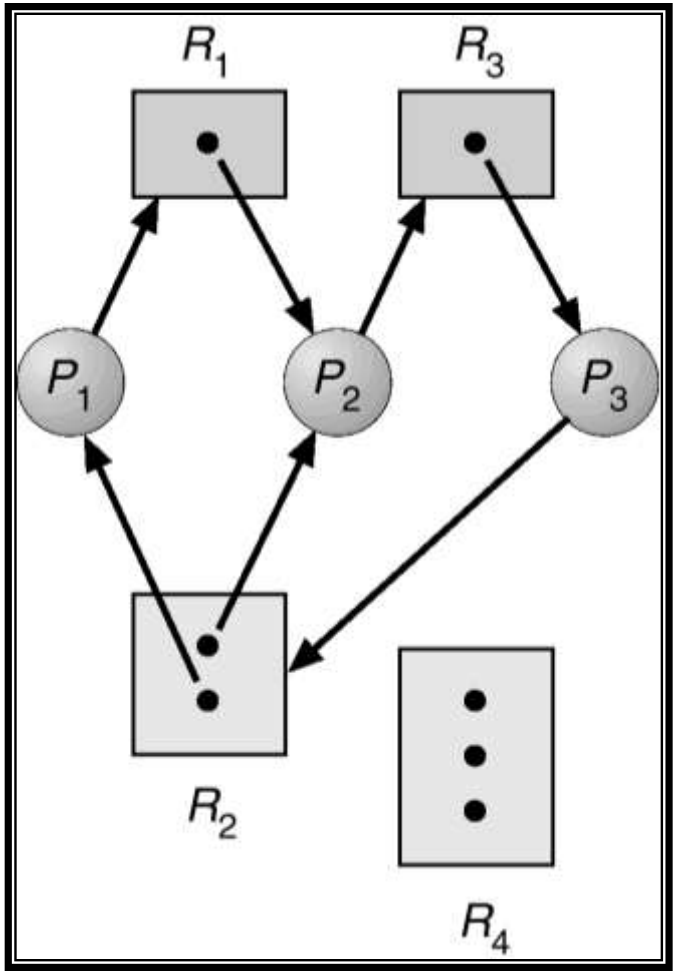
- P_i is holding an instance of R_i



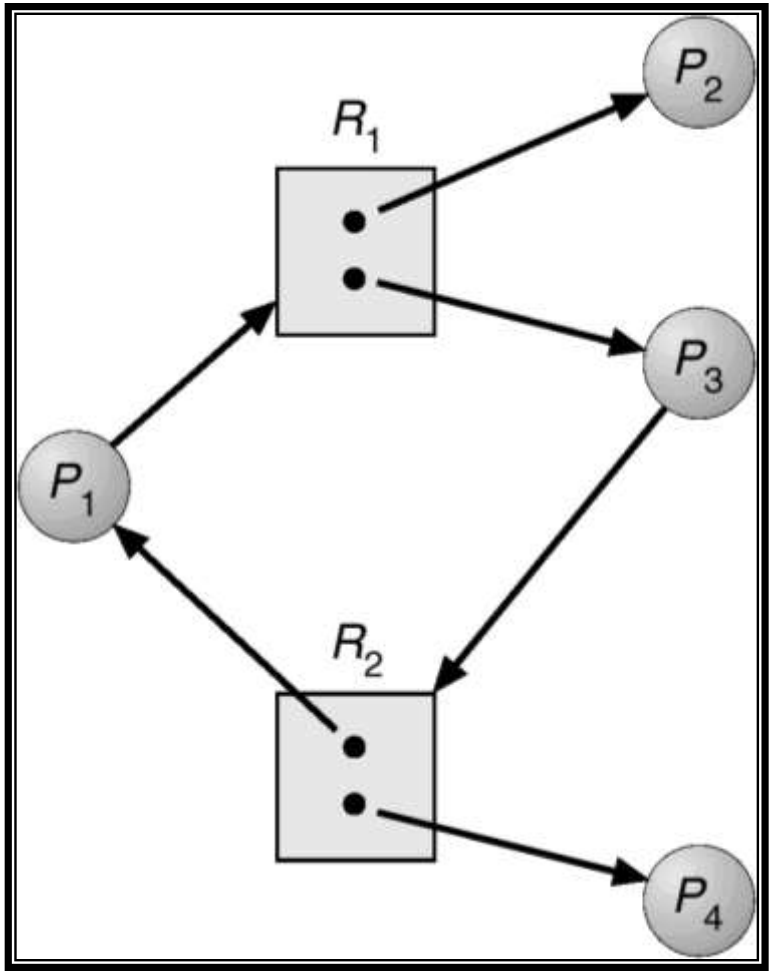
An Example of Resource Allocation Graph:



Resource Allocation Graph With Deadlock:



Resource Allocation Graph With No Deadlock:



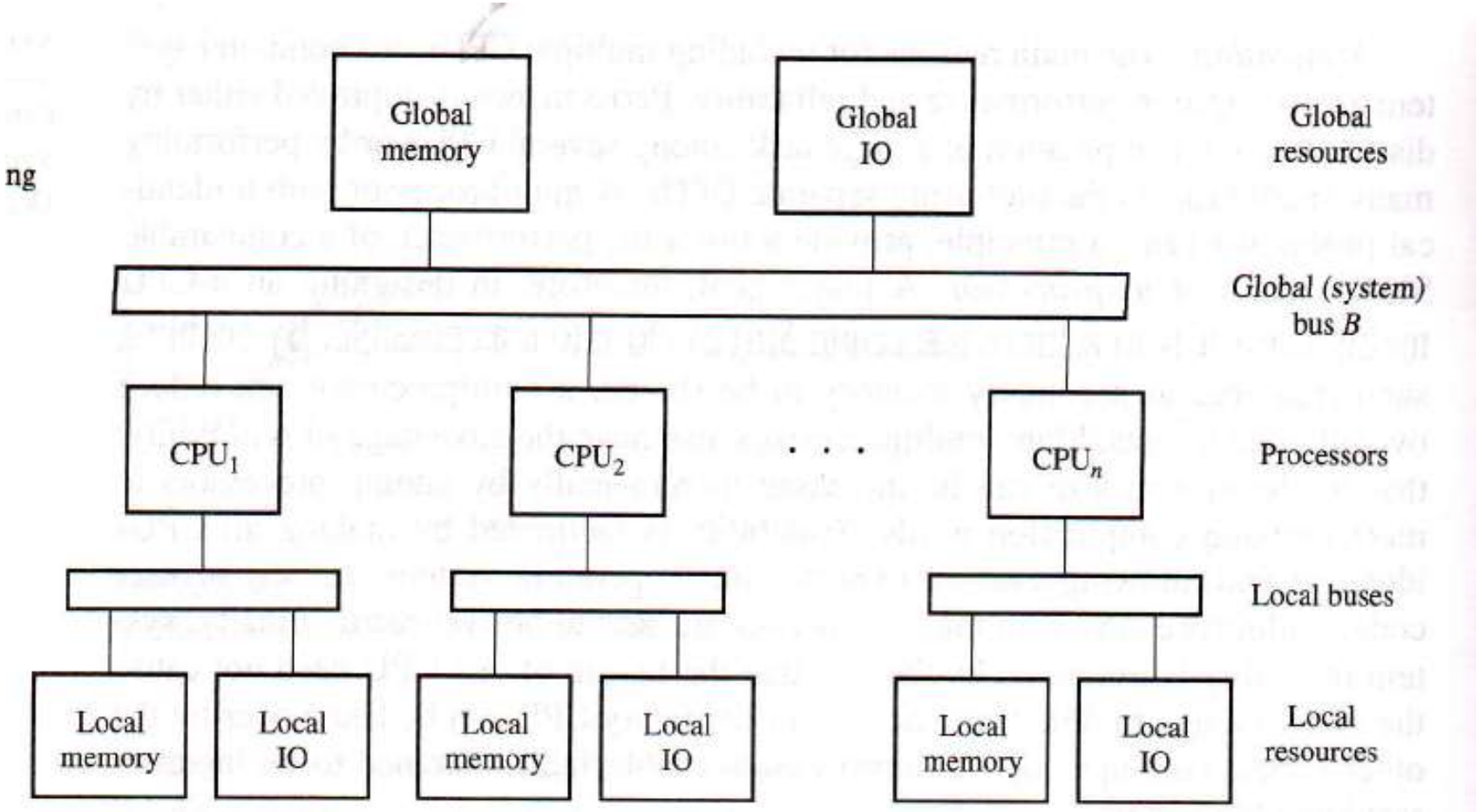
Parallel Processing

- Parallel processing is used to denote a large class of techniques that are used to provide simultaneous data processing task.

- There are two types of parallelism
  - Processor Level Parallelism
  - Instruction Level Parallelism

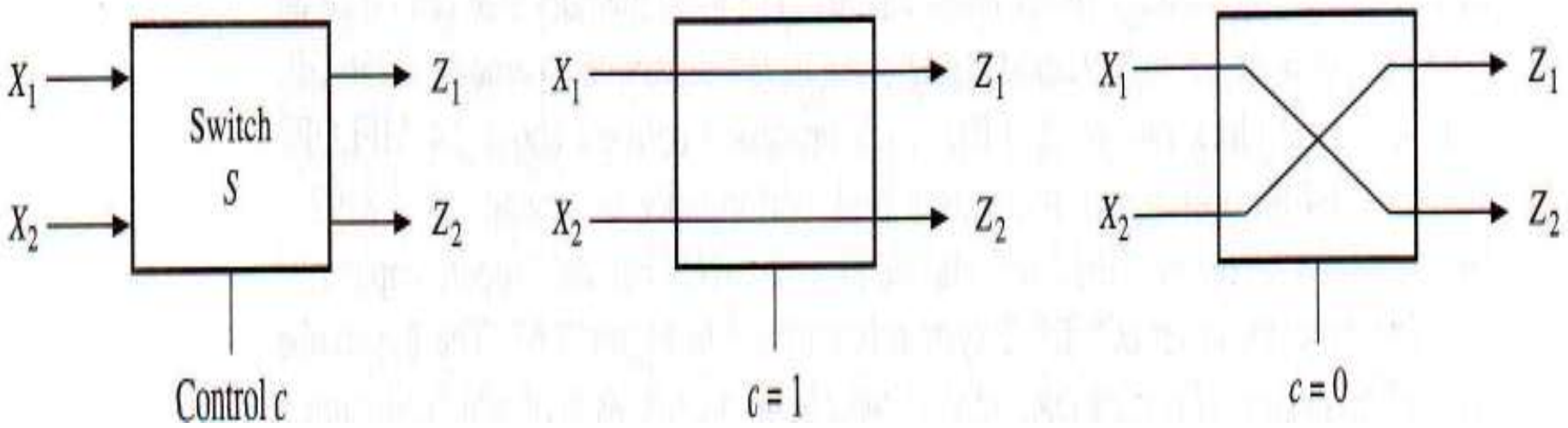
- Dependencies
- The Sequence of instructions read from memory constitutes an instruction stream. Parallel processing occur in both the instruction stream or in the data stream.
- Flynn's classified computer into 4 major groups:
  - SISD
  - SIMD
  - MISD
  - MIMD

- Multiprocessors :
  - Multiprocessor system are classified on two basis
    - Memory System
      - Shared memory-------tightly Coupled System
      - Distributed Memory------loosely Cpoupled System
    - Number of Processor
      - Massively Parallel
      - Modestly parallel
  - Uniform Access time


ng
Global memory
Global IO
Global resources
Global (system) bus B
CPU1
CPU2
. . .
CPUn
Processors
Local buses
Local memory
Local IO
Local memory
Local IO
Local memory
Local IO
Local resources

- Cache Coherence:-With an independent cache in each CPU, the possibility exists for two or more caches to contain different version of same information at the same time, this problem is known as cache coherence problem.
- We can solve this problem either by using two methods:
  - Hardware Based Methods
  - Software Based Methods

Multistage InterConnection Networks



An 8X8 Omega Multistage Interconnection Network: